DINGHUA TECHNOLOGY CO.,LTD

H6182P

Programmable Sound Generator

TEL:0755-83762717 FAX:0755-83762685

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1. Feature

- Built-in 8-bits MCU core (**JUPITER**).
- Built-in ***programmable sound generator*** (**PSG**)
- Built-in voltage control oscillator with *programmable* PLL (VCO-PLL clock generator).
- Internal system clock speed up to 45 MHz (max. 45 MHz at Vcc = 3.0V).
- Built-in 1Mbit (128K Bytes) OTP-ROM.
- Built-in 8Kbit (1024 Bytes) SRAM.
- Equipped 2 EQ-OP for signal amplifier or filter.
- Equipped 1 speaker amplifier (0.5W).
- Built-in 2-wired serial bus interface (I^2C like, slave mode).
- Built-in micro-controller interface (8-bit parallel interface).
- Equipped two (Left/Right audio) 16-bit DAC (voltage DAC) audio outputs.
- Analog Operating voltage (Vdd): 2.40V~4.50V (≥ Vcc).
- Digital Operating voltage (Vcc): 2.40V~3.60V (typ. 3.0V).
- Operating current: <20 mA (average operating current without audio load).
- Standby current: typ. 2.0 μA (25°C).
- Temperature Range : -45°C~85°C

2. Description

The H6182P series is based on 8-bit MCU (JUPITER) and equipped with a powerful programmable sound generator (PSG) for processing sweet-sounding. Via proprietary system bus, the MCU (JUPITER) features efficient addressing register and memory timing control register (MTR) to access internal/external memory and I/O devices with appropriate timing.

The H6182P is equipped with two high-resolution 16-bit D/A for audio output, which can support time-sharing mode for processing up to 64-poly sounds. There have been many firmware library of speech processing being implemented such as 4-bit ADPCM, 1-bit WFM, and so on. Since the H6161P has a built-in PSG, it also provides high quality standard MIDI playing library.

The H6182P features 24 general purpose I/O pins. Each can be individually programmed to input or output mode, and with internal pull-up or not. Each I/O of port 0 can be programmed to select interrupt source and the interrupt signal can be falling or rising trigger.

The H6182P features VCO and PLL to provide system clock. The frequency of the system clock is programmable up to 45 MHz. The device has two built-in 8-bit timers. Each timer is made up of an 8-bit up counter, 8-bit reload data, and pre-scale. Usually, the timer can be used to configure speech sampling frequency. The H6182P also supports two device interfaces: one is 2-wired serial bus, and the other is 8-bit parallel MCU control interface. The H6161P acts as a slave device and is able to communicate with the external host controller by either of the two interfaces.

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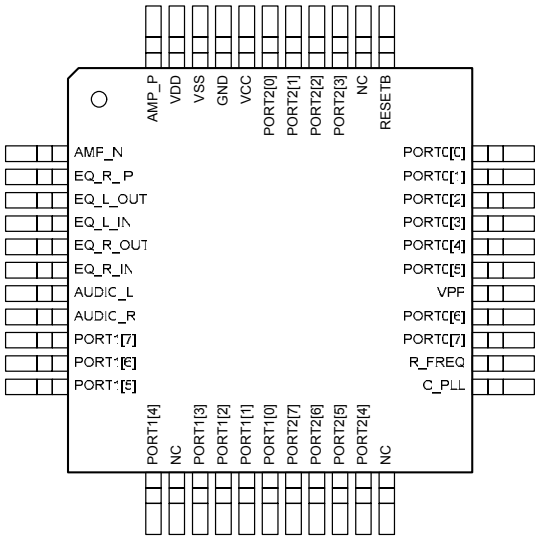
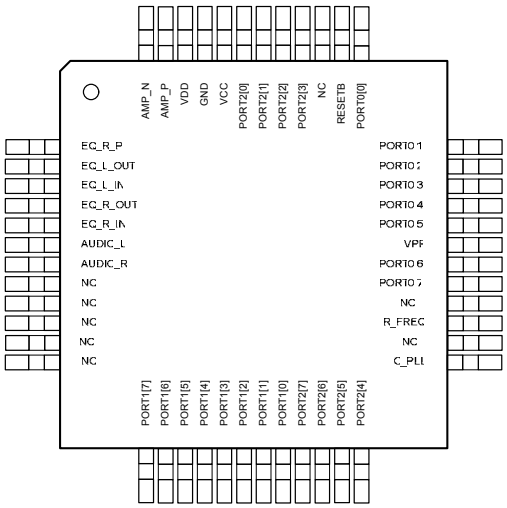
3. Pin Configurations



(QFP44 PACKAGE)



(LQFP48 PACKAGE)

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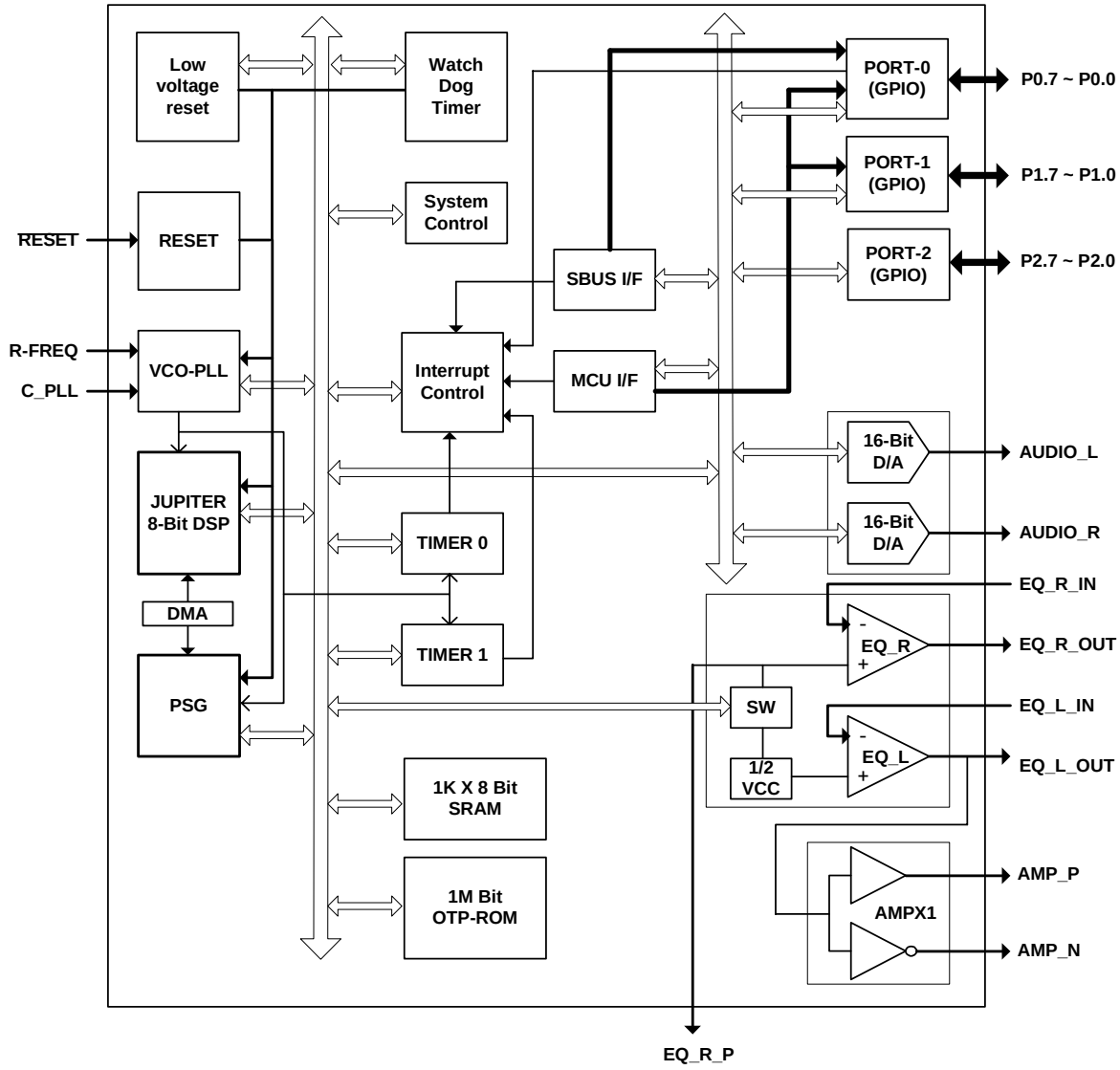
4. Block Diagram



H6182P Block Diagram

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5. Pins Function Definition

5.1. QFP44 Pins Function Definition

Pin No.	Designation	I/O	SMT	Description
1	AMP_N	A		Speaker amplifier negative output signal.
2	EQ_R_P	A		OP positive input/output in of EQ_R
3	EQ_L_OUT	A		OP out pin of EQ_L.
4	EQ_L_IN	A		OP negative input pin of EQ_L.
5	EQ_R_OUT	A		OP out pin of EQ_R.
6	EQ_R_IN	A		OP negative input pin of EQ_R.
7	AUDIO_L	A		16-bit D/A output of left audio.
8	AUDIO_R	A		16-bit D/A output of right audio.
9	P1[7] / MD7	I/O		Pin7 of general purpose I/O port 1 / data bus 7 of MCU I/F
10	P1[6] / MD6	I/O		Pin6 of general purpose I/O port 1 / data bus 6 of MCU I/F
11	P1[5] / MD5	I/O		Pin5 of general purpose I/O port 1 / data bus 5 of MCU I/F
12	NC			No connect
13	P1[4] / MD4	I/O		Pin4 of general purpose I/O port 1 / data bus 4 of MCU I/F
14	P1[3] / MD3	I/O		Pin3 of general purpose I/O port 1 / data bus 3 of MCU I/F
15	P1[2] / MD2	I/O		Pin2 of general purpose I/O port 1 / data bus 2 of MCU I/F
16	P1[1] / MD1	I/O		Pin1 of general purpose I/O port 1 / data bus 1 of MCU I/F
17	P1[0] / MD0	I/O		Pin0 of general purpose I/O port 1 / data bus 0 of MCU I/F
18	P2[7]	I/O		Pin7 of general purpose I/O port 2
19	P2[6]	I/O		Pin6 of general purpose I/O port 2
20	P2[5]	I/O		Pin5 of general purpose I/O port 2
21	P2[4]	I/O		Pin4 of general purpose I/O port 2
22	NC			No Connect
23	C_PLL	I		Input connecting external capacitor for DPLL
24	R_FREQ	I		Input connecting external resistor for base voltage control oscillator (VCO).
25	P0[7] / WRB	I/O		Pin7 of general purpose I/O port 0 / Write enable of MCU I/F
26	P0[6] / CSB	I/O		Pin6 of general purpose I/O port 0 / Chip select enable of MCU I/F
27	VPP	P		Digital power supply input: 2.6V~3.6V (Typ. 3.0V).
28	P0[5] / A0	I/O		Pin5 of general purpose I/O port 0 / A0 signal of MCU I/F
29	P0[4] / RDB	I/O		Pin4 of general purpose I/O port 0 / Read enable of MCU I/F
30	P0[3] / IRQ	I/O		Pin3 of general purpose I/O port 0 / Interrupt request input of MCU I/F
31	P0[2]	I/O		Pin2 of general purpose I/O port 0
32	P0[1] / SDA	I/O		Pin1 of general purpose I/O port 0 / 2-wired serial bus data pin
33	P0[0] / SCL	I/O		Pin0 of general purpose I/O port 0 / 2-wired serial bus clock pin
34	RESETB	I		Chip reset, low active.
35	NC			No Connect
36	P2[3]	I/O		Pin3 of general purpose I/O port 2
37	P2[2]	I/O		Pin2 of general purpose I/O port 2
38	P2[1]	I/O		Pin1 of general purpose I/O port 2
39	P2[0]	I/O		Pin0 of general purpose I/O port 2
40	VCC	P		Digital power supply input: 2.4V~3.6V (Typ. 3.0V).
41	GND	P		Ground
42	VSS	P		Analog ground
43	VDD	P		Analog power supply input
44	AMP_P	A		Speaker amplifier positive output signal.

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5.2. LQFP48 Pins Function Definition

Pin No.	Designation	I/O	Description
1	EQ_R_P	A	OP positive input/output in of EQ_R
2	EQ_L_OUT	A	OP out pin of EQ_L.
3	EQ_L_IN	A	OP negative input pin of EQ_L.
4	EQ_R_OUT	A	OP out pin of EQ_R.
5	EQ_R_IN	A	OP negative input pin of EQ_R.
6	AUDIO_L	A	16-bit D/A output of left audio.
7	AUDIO_R	A	16-bit D/A output of right audio.
8	NC		
9	NC		
10	NC		
11	NC		
12	NC		
13	P1[7] / MD7	I/O	Pin7 of general purpose I/O port 1 / data bus 7 of MCU I/F
14	P1[6] / MD6	I/O	Pin6 of general purpose I/O port 1 / data bus 6 of MCU I/F
15	P1[5] / MD5	I/O	Pin5 of general purpose I/O port 1 / data bus 5 of MCU I/F
16	P1[4] / MD4	I/O	Pin4 of general purpose I/O port 1 / data bus 4 of MCU I/F
17	P1[3] / MD3	I/O	Pin3 of general purpose I/O port 1 / data bus 3 of MCU I/F
18	P1[2] / MD2	I/O	Pin2 of general purpose I/O port 1 / data bus 2 of MCU I/F
19	P1[1] / MD1	I/O	Pin1 of general purpose I/O port 1 / data bus 1 of MCU I/F
20	P1[0] / MD0	I/O	Pin0 of general purpose I/O port 1 / data bus 0 of MCU I/F
21	P2[7]	I/O	Pin7 of general purpose I/O port 2
22	P2[6]	I/O	Pin6 of general purpose I/O port 2
23	P2[5]	I/O	Pin5 of general purpose I/O port 2
24	P2[4]	I/O	Pin4 of general purpose I/O port 2
25	C_PLL	I	Input connecting external capacitor for DPLL
26	NC		
27	R_FREQ	I	Input connecting external resistor for base voltage control oscillator (VCO).
28	NC		
29	P0[7] / WRB	I/O	Pin7 of general purpose I/O port 0 / Write enable of MCU I/F
30	P0[6] / CSB	I/O	Pin6 of general purpose I/O port 0 / Chip select enable of MCU I/F
31	VPP/VSL	P	Digital power supply input: 2.6V~3.6V (Typ. 3.0V).
32	P0[5] / A0	I/O	Pin5 of general purpose I/O port 0 / A0 signal of MCU I/F
33	P0[4] / RDB	I/O	Pin4 of general purpose I/O port 0 / Read enable of MCU I/F
34	P0[3] / IRQ	I/O	Pin3 of general purpose I/O port 0 / Interrupt request input of MCU I/F
35	P0[2]	I/O	Pin2 of general purpose I/O port 0
36	P0[1] / SDA	I/O	Pin1 of general purpose I/O port 0 / 2-wired serial bus data pin
37	P0[0] / SCL	I/O	Pin0 of general purpose I/O port 0 / 2-wired serial bus clock pin
38	RESETB	I	Chip reset, low active.
39	NC		
40	P2[3]	I/O	Pin3 of general purpose I/O port 2
41	P2[2]	I/O	Pin2 of general purpose I/O port 2
42	P2[1]	I/O	Pin1 of general purpose I/O port 2
43	P2[0]	I/O	Pin0 of general purpose I/O port 2
44	VCC	P	Digital power supply input: 2.4V~3.6V (Typ. 3.0V).
45	GND	P	Ground
46	VDD	P	Analog power supply input
47	AMP_P	A	Speaker amplifier positive output signal.
48	AMP_N	A	Speaker amplifier negative output signal.

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6. Electrical Specifications

6.1. Recommend Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC, VPP	Digital Power Supply Voltage	-0.3	3.0	3.4	V
T_{OP}	Operating Temperature	-45	-	85	℃
T_{STG}	Storage Temperature	-45	-	125	℃
V_{DCIN}	DC Input Voltage	-0.3	-	VCC+0.3V	V
VDD	Analog Power Supply Voltage	VCC	VCC	VCC+0.3V	V
F_{BCLK} (RC_{OSC})	Base Clock Frequency	1.20-0.5%	1.20	1.20+0.5%	MHz@3.0V
F_{OSC}($DPLL_{OSC}$)	DPLL Clock (System Clock) Frequency	20	40	45	MHz@3.0V

6.2. DC Electrical Characteristics

(Vcc=V_{DD} = 3.0V, V_{SS} = 0V, F_{OSC} = 45 MHz, TA = 25℃, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
P0[0..7] P1[0..7] P2[0..7]	Driving Current	-	4	4	mA	V_{OH}=2.7V For each I/O
AUDIO_L AUDIO_R EQ_L_OUT EQ_R_OUT	Driving Current	-	4	4	mA	V_{OH}=2.7V
AMP_P AMP_N	Driving Current	-	-	250	mA	RL=8Ω , V_{OH}=2.3V Speaker Loading
P0[0..7] P1[0..7] P2[0..7]	Sink Current	-	4	4	mA	V_{OL}=0.3V For each I/O
AUDIO_L AUDIO_R EQ_L_OUT EQ_R_OUT	Sink Current	-	4	4	mA	V_{OL}=0.3V
AMP_P AMP_N	Sink Current	-	-	250	mA	RL=8Ω , V_{OL}=0.7V Speaker Loading
I_{STB}	Standby Current	1.2 -	1.5 -	2 3	uA	VCC=VDD=3.0V VCC=VDD=3.6V
I_{OP}	Operating Current	13	-	17	mA	1. Minimum @CPU wait (WAIT instruction) 2. Maximum @CPU operating All condition: PSG on DAC on EQ-OP on AMP on , without Load F_{OSC} = 45MHz
I_{TS}	Total I/O Sink Current	-	50	50	mA	V_{OL}=0.3V
I_{TD}	Total I/O Driving Current	-	40	40	mA	V_{OH}=2.7V

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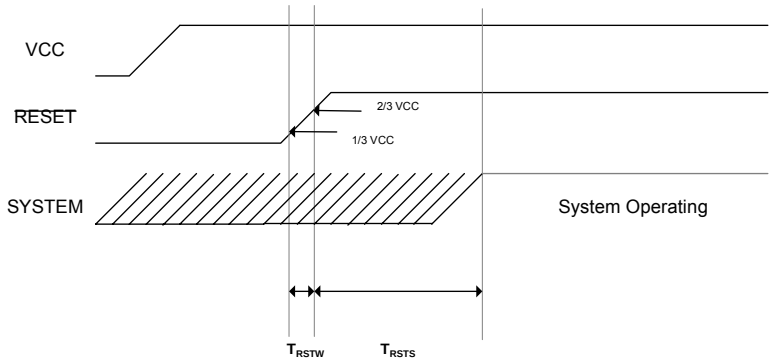
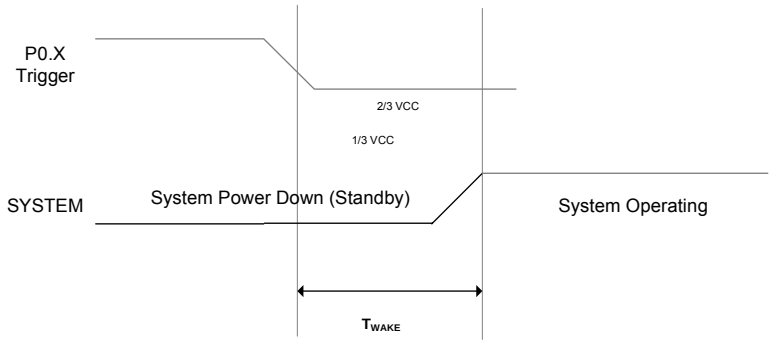
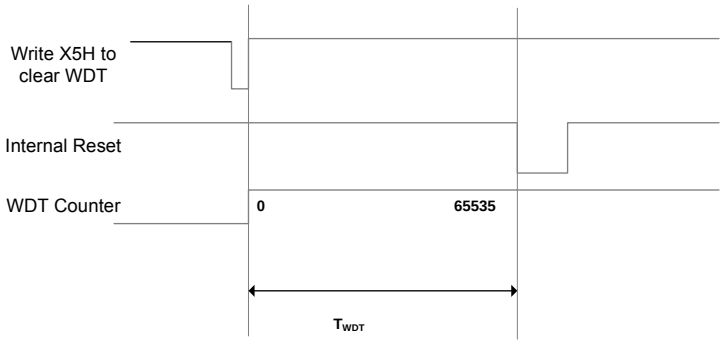
6.3. AC Electrical Characteristics

RESET

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RSTW}	Reset pulse width (Low pulse)	100	100	-	us
T_{RSTS}	Reset setup time	1	1	1.5	ms
T_{WAKE}	Wakeup time	0.4	-	1.5	ms
T_{WDT}	Watch Dog Timer	54.395	-	870	ms







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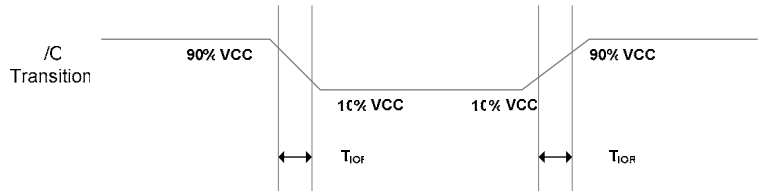
6.4. Switch Characteristics of MCU Interface

MCU Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TAS	Address Set-Up Time	0	-	-	nS	Configure the MCU interface to enable
TAH	Address Hold time	0	-	-	nS	
TDS	Data Set-Up Time	20	-	-	nS	
TDH	Data Hold time	2	-	-	nS	
TAC	Access Time	0	-	-	nS	
TPW	Pulse Width time	20	-	-	nS	

Switch Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
F_{BCLK} (RC_{OSC})	Base Clock Frequency	1.15	1.20	1.26	**MHz**	VCC@3.0V R_{FREQ}=270KΩ
F_{OSC}($DPLL_{OSC}$)	System Clock Frequency	DPLL_CONTROL x F_{BCLK}				1. Minimum DPLL_CONTROL=C0H 16.13 x F_{BCLK} 2. Maximum DPLL_CONTROL=38H 37.00 x F_{BCLK}
T_{IOR}	I/O output transition rising time	45	-	-	ns	No Load (10% to 90%)
T_{IOF}	I/O output transition falling time	45	-	-	ns	No Load (10% to 90%)



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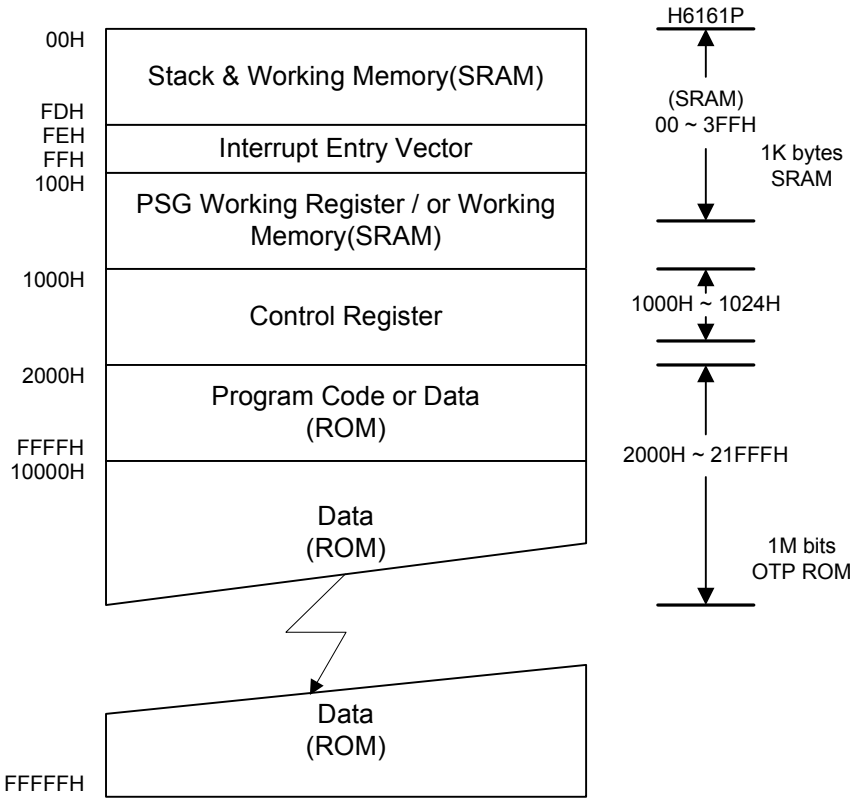
7. Memory and Control Registers Architecture

The following are memory in H6182P platform

(1) Control registers (decode space 1000H ~ 101FH)
(2) SRAM (access time: Max. 12 ns, condition typ. Vcc = 3.0V)
(3) ROM (access time: Max. 90 ns, condition typ. Vcc = 3.0V)

The program code starting address is 2000H after system reset, and the program code runs within front 64K bytes (the CPU JUPITER program counter (PC) is 16 bits). The constant data can be stored in any place of ROM space.

7.1. Memory Map



Memory and Register Map

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7.2. Control Registers Summary Table

H6182P Control Registers Summary

Address (Hex)	Simplified Name	Complete Name	Register Function Brief
1000	**SCR**	System Control Register	Speaker Amplifier on/off, Equalizer EQs on/off, DAC output on/off, SBUS I/F enable/disable, MCU I/F enable/disable, PSG on/off, System clock on/off.
1001	**IRQER**	Interrupt Request Enable Register	Interrupt control register, enable/disable MCU/SBUS/TIMER0/TIMER1/PORT0 interrupts.
1002	**IRQSR**	Interrupt Status Register	Interrupt Status, to indicate the status of MCU/SBUS/TIMER0/TIMER1/PORT0 interrupts.
1003	**DPLLR**	DPLL Control Register	Configure for system clock.
1004 1005	**LDACR**	Left DAC Register	16-bit DAC output control register
1006 1007	**RDACR**	Right DAC Register	16-bit DAC output control register
1008	**PSGCR**	PSG Control Register	PSG control register
1009	**PSGMTR**	PSG Memory Timing Register	PSG memory access timing control.
100A	**PSGVR**	PSG Volume Register	PSG volume control register
100B	**PSGMIX**	PSG Mixing Rate Register	PSG mixing-rate control register
100C	**TMR**	Timer Control Register	Timer 0/1 counter enable/disable, pre-scale clock select.
100D	**T0RR**	Timer 0 Reload Register	Set reload value of timer 0 counter.
100E	**T0DR**	Timer 0 Data Register	Set value of timer 0 counter or get current count value of timer 0.
100F	**T1RR**	Timer 1 Reload Register	Set reload value of timer 1 counter.
1010	**T1DR**	Timer 1 Data Register	Set value of timer 1 counter or get current count value of timer 1.
1011	**P0IMR**	Port 0 Interrupt Mask Register	Enable/disable each port 0 input interrupt source
1012	**P0IPR**	Port 0 Interrupt Polarity Register	Select interrupt trigger condition, falling or rising edge.
1013	**P0ISR**	Port 0 Interrupt Status Register	Indicate the port 0 interrupt asserted or not.
1014	**P0MR**	Port 0 I/O Mode Register	Select the I/O direction of port 0.
1015	**P0PR**	Port 0 Pull-up Control Register	Select port 0 I/O pull-up resistor.
1016	**P0DR**	Port 0 Data Register	Set the port 0 output data/ fetch logical values of port 0 pins.
1017	**P1MR**	Port 1 I/O Mode Register	Select the I/O direction of port 1.
1018	**P1PR**	Port 1 Pull-up Control Register	Select port 1 I/O pull-up resister.
1019	**P1DR**	Port1 Data Register	Set the port 1 output data/ fetch logical values of port 0 pins.
101A	**MCUSR**	MCU Status Register	Indicate command or data read/write of MCU I/F.
101B	**MCUDR**	MCU Data Register	MCU data exchange data buffer
101C	**SBUSMR**	SBUS Mode Register	Transfer complete status, bus status, general call status, 1st write data (1st receive data), read/write status (direction).
101D	**SBUSSR**	SBUS Status Register	2-wired serial bus status register
101E	**SBUSTX**	SBUS Transmit Register	2-wired serial bus transmit data register
101F	**SBUSRX**	SBUS Receive Register	2-wired serial bus receive data register
1020	**ACR**	Advance Control Register	System clock fast/slow, LVD enable/disable, EQ_R_P free/connect to H_VCC
1021	**WDTC**	Watch Dog Control Register	Disable/Enable/Clear the Watch Dog Timer
1022	**P2MR**	Port 2 I/O Mode Register	Set the port 2 I/O direction.
1023	**P2PR**	Port 2 Pull-up Control Register	Select port 2 I/O pull-up register or not.
1024	**P2DR**	Port 2 Data Register	Set the port 2 output data, or get the port 2 pin logical.

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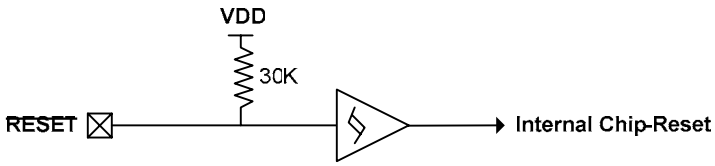
8. Control Registers Description

8.1. System Reset

The occurrence of H6182P reset causes all the control registers to be set to default values, and the DSP-core (Jupiter) is also restarted and begins to execute the program from the address 2000H.

There are some errata should be took care after the system reset, because the VCO-DPLL is not so stable while the reset occurs. Thus, to wait the system clock stable is necessary in this version of H6182P.



The System Reset Block Diagram

The following is the reference code used to wait the system clock to be stable after system reset, it is also used after the system is waked-up from power down mode.

```
WAIT_CLOCK_STABLE       FUNCTION

                        PUSH    PSR
                        CLI
                        PUSH    [IRQ_ENABLE]                    ; BACKUP IRQ_ENABLE
                        PUSH    [TIMER_CONTROL]                 ; BACKUP TIMER_CONTROL
                        PUSH    [TIMER1_RELOAD]                 ; BACKUP TIMER1_RELOAD
                        PUSH    [TIMER1_DATA]                   ; BACKUP TIMER1_DATA
                        PUSHW   [IRQ_VECTOR]                    ; BACKUP IRQ_VECTOR
                        ; ---------------------------------------
                        MOVE    [TIMER1_DATA], 0                ; RESET TIMER VALUE
                        MOVE    [TIMER1_RELOAD], (2 / (1000/(BASE_CLOCK/64)))-1
                        MOVE    [TIMER_CONTROL], 10100000B      ; ENABLE T1(BASE_CLOCK/64)
                        MOVE    [IRQ_ENABLE], 00000010B         ; ONLY ENABLE T1
                        MOVE    [IRQ_STATUS], 11111100B         ; T0,T1 ISR EOI
                        MOVEW   [IRQ_VECTOR], WAIT_STABLE_T1_ISR ; REDIRECT ISR ENTRY
                        STI
                        WAIT                                    ; WAIT 2 ms INTERRUPT
                        CLI
                        ; ---------------------------------------
                        POPW    [IRQ_VECTOR]                    ; RESTORE IRQ_VECTOR
                        POP     [TIMER1_DATA]                   ; RESTORE TIMER1_DATA
                        POP     [TIMER1_RELOAD]                 ; RESTORE TIMER1_RELOAD
                        POP     [TIMER_CONTROL]                 ; RESTORE TIMER_CONTROL
                        POP     [IRQ_ENABLE]                    ; RESTORE IRQ_ENABLE
                        POP     PSR
                        RET
                        ; ---------------------------------------

WAIT_STABLE_T1_ISR
                        MOVE    [IRQ_STATUS],11111101B          ; T1 ISR EOI
                        RETI

WAIT_CLOCK_STABLE       ENDF
```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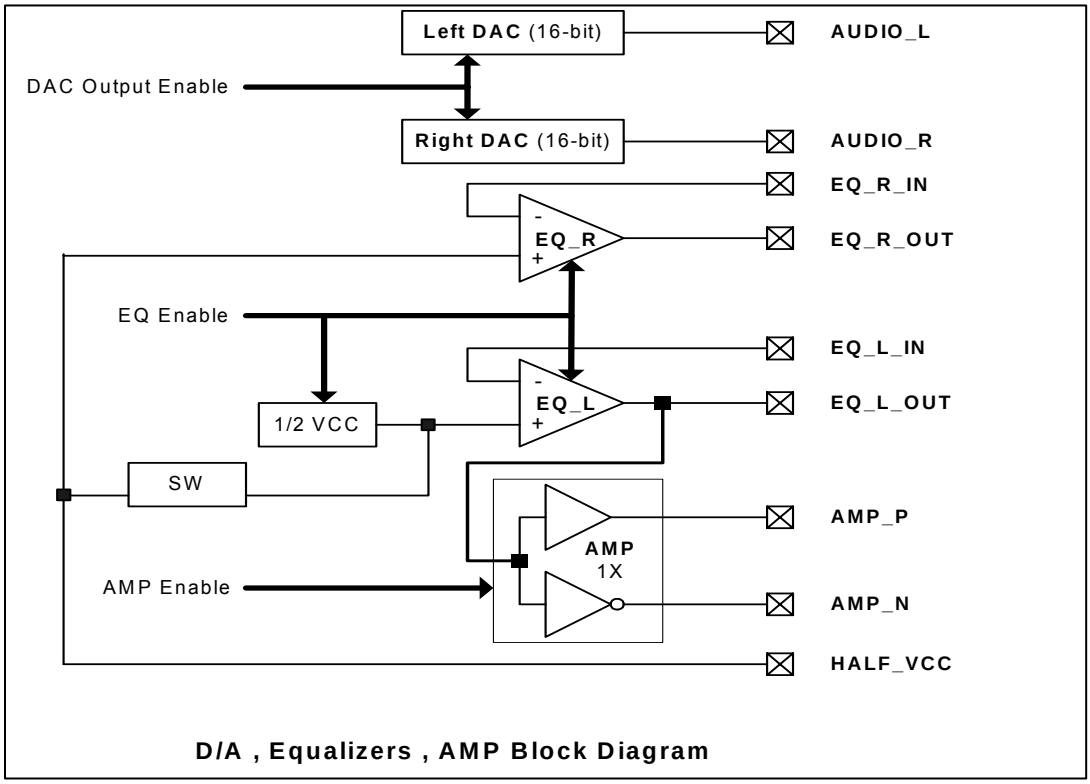
8.2. System Equipment Control (16-Bit DAC, EQ-OP & AMP)

The H6182P has the following equipments and functions:

(1) AMP (Speaker Amplifier)
(2) EQ_L (equalizer OP)
(3) EQ_R (equalizer OP)
(4) MCU (8-bit parallel data bus) interface
(5) SBUS (2-wired serial bus) interface
(6) PSG (Programmable Sound Generator)
(7) VCO-DPLL (Programmable system oscillator)
(8) General Purpose I/O , Port-0 and Port-1 and Port-2



D/A , Equalizers , AMP Block Diagram

1000H: System Control Register (SCR)

1000H , System Control Register (SCR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Clock On/Off	PSG On/Off	MCU I/F On/Off	SBUS I/F On/Off	DAC Output On/Off	EQ-OP On/Off	Speaker Amplifier On/Off	Reserved
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

The system control register is defined to control the equipments and function blocks to enable or disable.

BIT 7: Clock On/Off
0: System clock is off.
1: System clock is on.

BIT 6: PSG On/Off
0: PSG is off.
1: PSG is on.

BIT 5: MCU Interface On/Off
0: MCU interface disable.

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1: MCU interface enable.

BIT 4: SBUS interface On/Off (2-wired serial bus)
0: SBUS interface disable.
1: SBUS interface enable.

BIT 3: D/A Output On/Off
0: D/A output (AUDIO_L / AUDIO_R) disable
1: D/A output (AUDIO_L / AUDIO_R) enable

BIT 2: EQ-OP and 1/2 VCC On/Off
0: The EQ-OP (equalizers) is off.
1: The EQ-OP (equalizers) is on.

BIT 1: Speaker Amplifier On/Off
0: The speaker amplifier is off.
1: The speaker amplifier is on.

The following is the example code to control the speaker amplifier on/off procedures for getting ready to start outputting D/A signal or stopping the output.

```
; ================================================================================
AMP_ON_PROC     FUNCTION
                MOVE    AX, 8000H
                MOVE    [LEFT_DAC], AX                  ; LEFT_DAC = SILENCE LEVEL.
                MOVE    [RIGHT_DAC], AX                 ; RIGHT_DAC= SILENCE LEVEL.
                NOP
                NOP
                OR      [SYSTEM_CONTROL], 00001000B     ; DAC ON.
                NOP
                OR      [SYSTEM_CONTROL], 00001100B     ; EQ  ON.
                NOP
                OR      [SYSTEM_CONTROL], 00001110B     ; AMP ON.
                RET
AMP_ON_PROC     ENDF
; ================================================================================
AMP_OFF_PROC    FUNCTION
                AND     [SYSTEM_CONTROL], 11111101B     ; AMP OFF.
                NOP
                AND     [SYSTEM_CONTROL], 11111001B     ; EQ  OFF.
                NOP
                AND     [SYSTEM_CONTROL], 11110001B     ; DAC OFF.
                NOP
                NOP
                MOVE    AX,0000H
                MOVE    [LEFT_DAC],AX
                MOVE    [RIGHT_DAC], AX
                RET
AMP_OFF_PROC    ENDF
; ================================================================================
```


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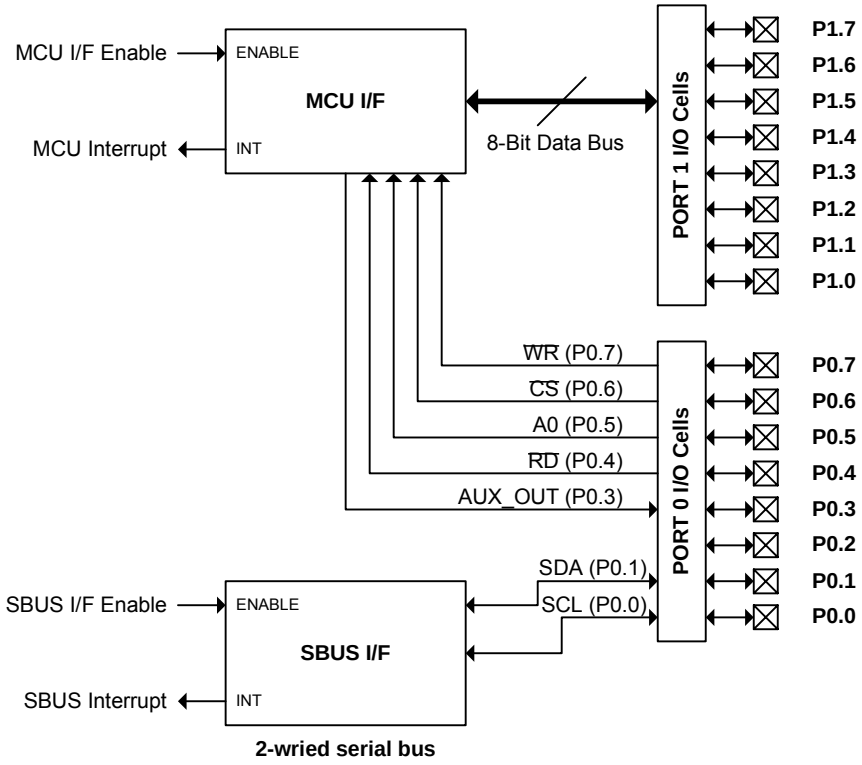
The H6182P supports two communication function blocks, one is 8-bit parallel MCU interface and the other is 2-wired serial bus. In most part of cases, the H6182P is configured to be a slave sound device, so these two functions are very useful to interface with most parts of MCU system.



MCU I/F , SBUS I/F , Port I/O Functions Block Diagram

The H6182P is based on 8-bit DSP core name "JUPITER", and a powerful programmed sound generator is embedded to process the 24-poly sounds that are also called as wave-table processor.

In order to process 24 different sounds at the same time, the H6182P supports a VCO-DPLL function to generate a high and stable system clock, and this VCO-DPLL is programmable to fit the different application.

8.3. System Clock Control (VCO-DPLL)

1003H: DPLL Control Register (DPLLR)

1003H ,DPLL Control Register (DPLLR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	DPLL Divider Factor		DPLL Multiply Factor					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	1	1

Set this register to control the system clock speed.
The default value 10001011b (8BH) will set the system clock to (20 x base clock).
Typically: base clock = 1.2MHz, Vcc = 3.3V, R_FREQ = 270KΩ.
After power on reset, system clock = 20.00 x 1.200MHz = 24.00 MHz.

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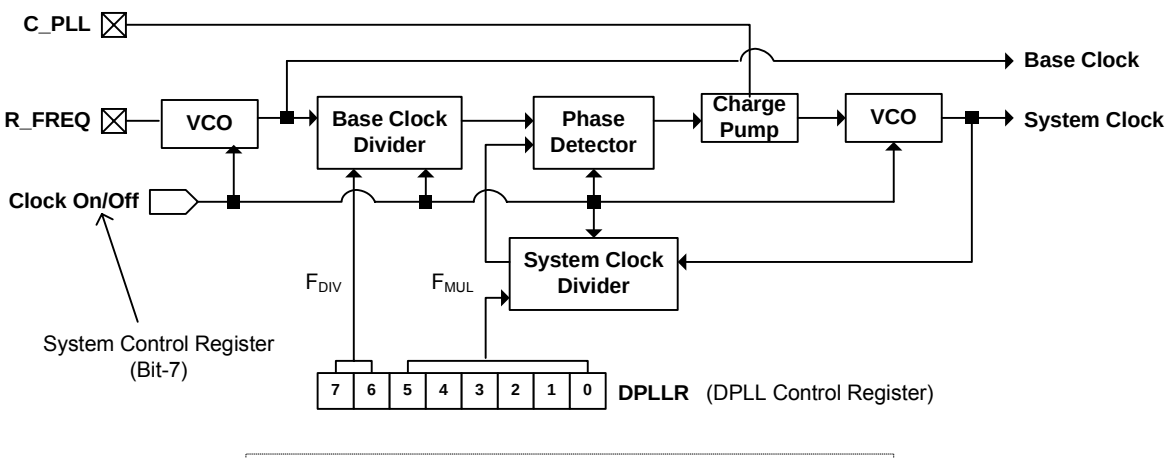


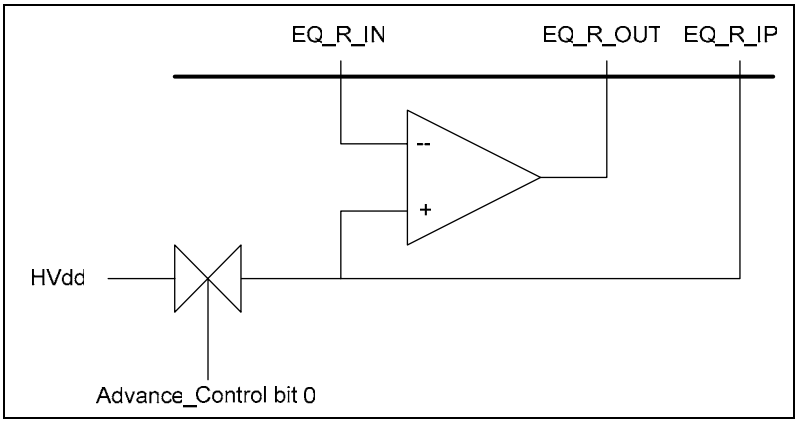
$$\text{System Clock} = \frac{F_{MUL} + 129}{F_{DIV} + 5} \times \text{Base Clock}$$

VCO-DPLL Functional Block Diagram

1020H: Advanced Control Register (ACR)

1020H , Advanced Control Register (ACR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved					CPU Operate Speed	LVD Enable/Disable	HVdd Enable/Disable
Read/Write	X	X	X	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	0	1	1	1	0

[2] CPU operates speed:
1 = CPU operate in high speed (default),
0 = CPU operate in low speed (1.2Mhz)
[1] Low Voltage Detect: This bit is set to enable the low voltage reset function
1 = Enable. (Default)
0 = Disable.
[0] HVdd Enable/Disable: This bit is set EQ-R-IP to enable HVdd output.
1 = Enable.
0 = Disable.



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8.4. Programmable Sound Generator (PSG)

The programmed sound generator features wave-table process unit that supports ADSR envelops function to emulate the music instrument sounding, and mixes multi-channels sounds by setting parameters to each PSG working registers.

Thus, just program the music sequencer firmware for JUPITER DSP core, and constructs the instrument wave data, the H6182P can present sweet and high quality music, it can be called melody-chip, MIDI-chip, and power music synthesizer.

The PSG function uses the DMA (direct memory access) architecture to co-process with the JUPITER DSP core.

1008H: PSG Control Register (PSGCR)

1008H , PSG Control Register (PSGCR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PSG D/A Mode	D/A Level Mode	PSG channel number					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7: PSG D/A output mode

0: Update D/A with time-sharing mode.

1: Update D/A with summation mode.

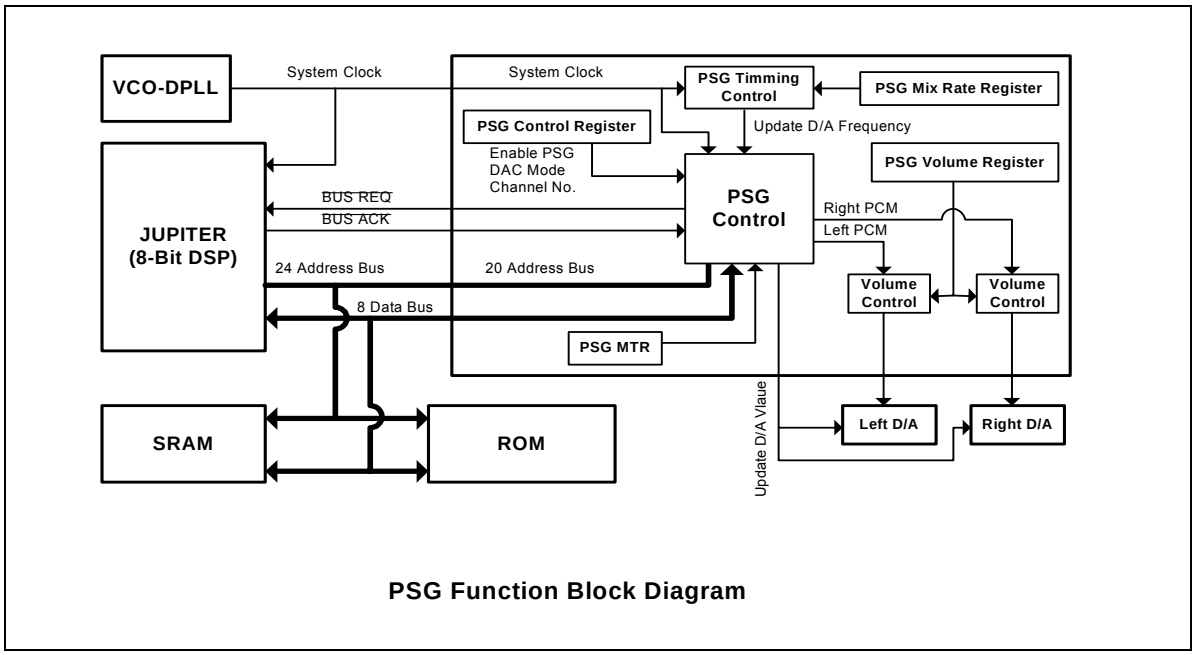
BIT 6: PSG D/A output level mode

0: The minimum D/A output level is 0.

1: The minimum D/A output level is 1/4 Vcc.

BIT 5~0: PSG channel number setting

Set this number to define the PSG channel number, for example, if this value is 23, the PSG will process 24 channels mixing. In other word, to process N channels, write (N-1) to these 6 bits.



PSG Function Block Diagram

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1009H: PSG Memory Timing Register (PSGMTR)

1009H ,PSG Memory Timing Register (PSGMTR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name				Wave table access wait clocks			PSG SRAM wait clocks	
Read/Write	X	X	X	W	W	W	W	W
Reset	X	X	X	0	0	0	0	0

The PSGMTR is defined to control the timing of memory access, its operation is similar to the JUPITER's MTR.
BIT 4~2: Set the accessing time of wave-table (ROM) to wait 0~7 system clock cycles.
BIT 1~0: Set the accessing time of PSG working registers (SRAM) to wait 0~3 system clock cycles.

100AH: PSG Volume Control Register (PSGVR)

100AH ,PSG Volume Control Register (PSGVR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PSG Volume							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Set this register to control the PSG volume level from 0 ~ 255.

$$\text{Left/Right DAC output value (16-Bit)} = \frac{\text{PSG volume}}{256} \times \text{PSG Left/Right PCM value}$$

100BH: PSG Mix Rate Control Register (PSGMIX)

100BH ,PSG Mix Rate Control Register (PSGMIX)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PSG Mix Rate Factor							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Set this register to control the frequency of PSG updating DAC output.

$$\text{Mix Rate Factor} = \frac{\text{System Clock}}{\text{Mix Rate}} \Big/ \text{PSG channel number}$$

For example, if the system clock is 45000000Hz, mixing rate is 44100Hz, and PSG channel number is 24. Then the "Mix Rate Factor" is (45000000/44100)/24 = 42 (2AH).

Note that this value can not be less than 31 (1FH) because of the PSG DMA clock phase, this is undocumented.

About PSG Working Registers

The PSG working registers are mapped overlapping with the SRAM (working memory) and the 1st working register of the 1st channel starts from address **100H** (please refer to the memory and register map).

Since these working registers are accessed by both DSP-Core (Jupiter) and PSG, the PSG uses the DMA bus to sharing the controlling with the Jupiter.

Each channel of PSG contains **16** bytes working registers, they are defined to control the sounding value and operation for each channel. Therefore, there are 384(16 x 24) bytes totally for controlling 24 channels sounding.

The following table shows the structure of working registers for each channel of PSG:

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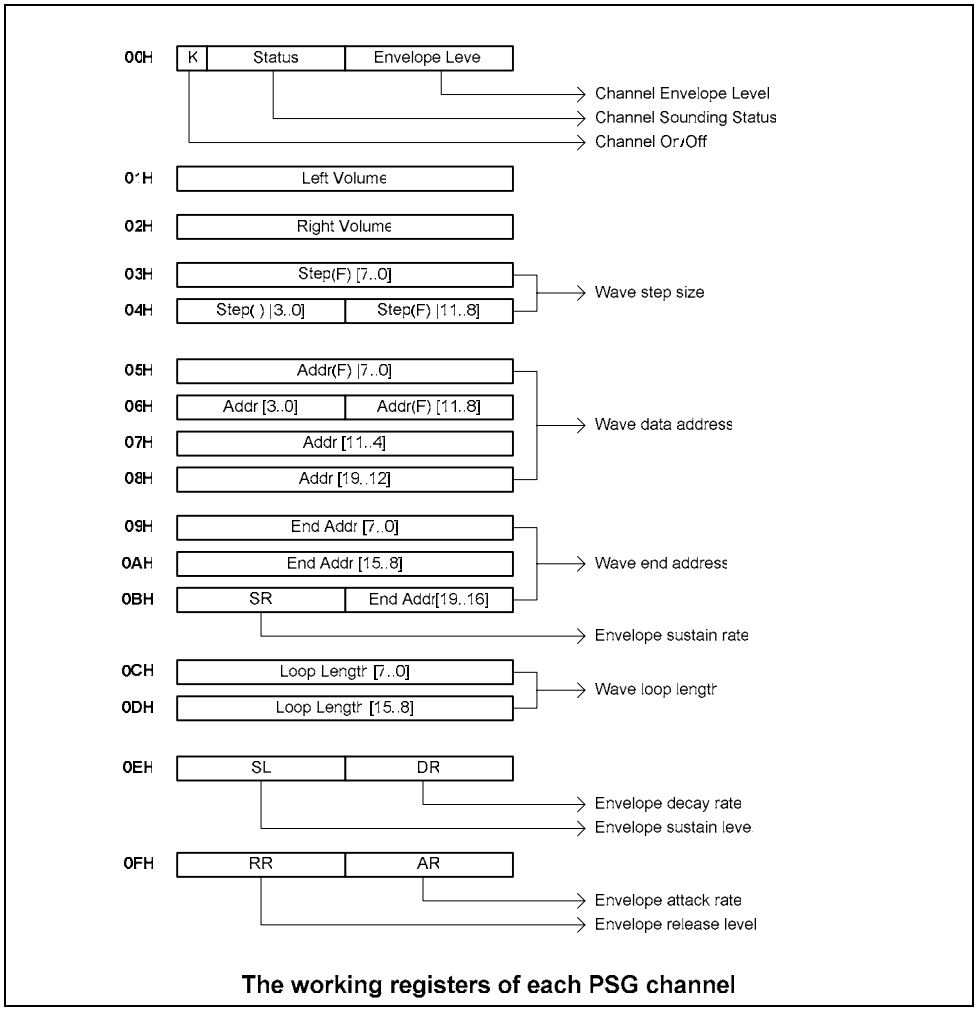
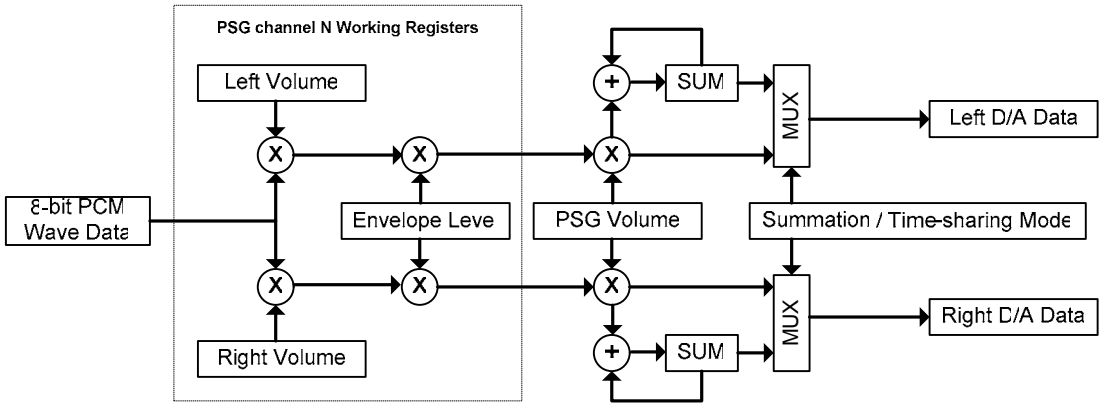


The working registers of each PSG channel

The PSG of H6182P supports 3 volume control units:

(1) Envelope level (4 bits), ADSR envelope controlling.
(2) Left / Right channel volume (8 bits), stereo audio output supporting.
(3) PSG volume (8 bit), this also named global output volume.



The PSG Volume Control

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8.5. General Purpose Input/Output Control, GPIO Port0, 1, 2

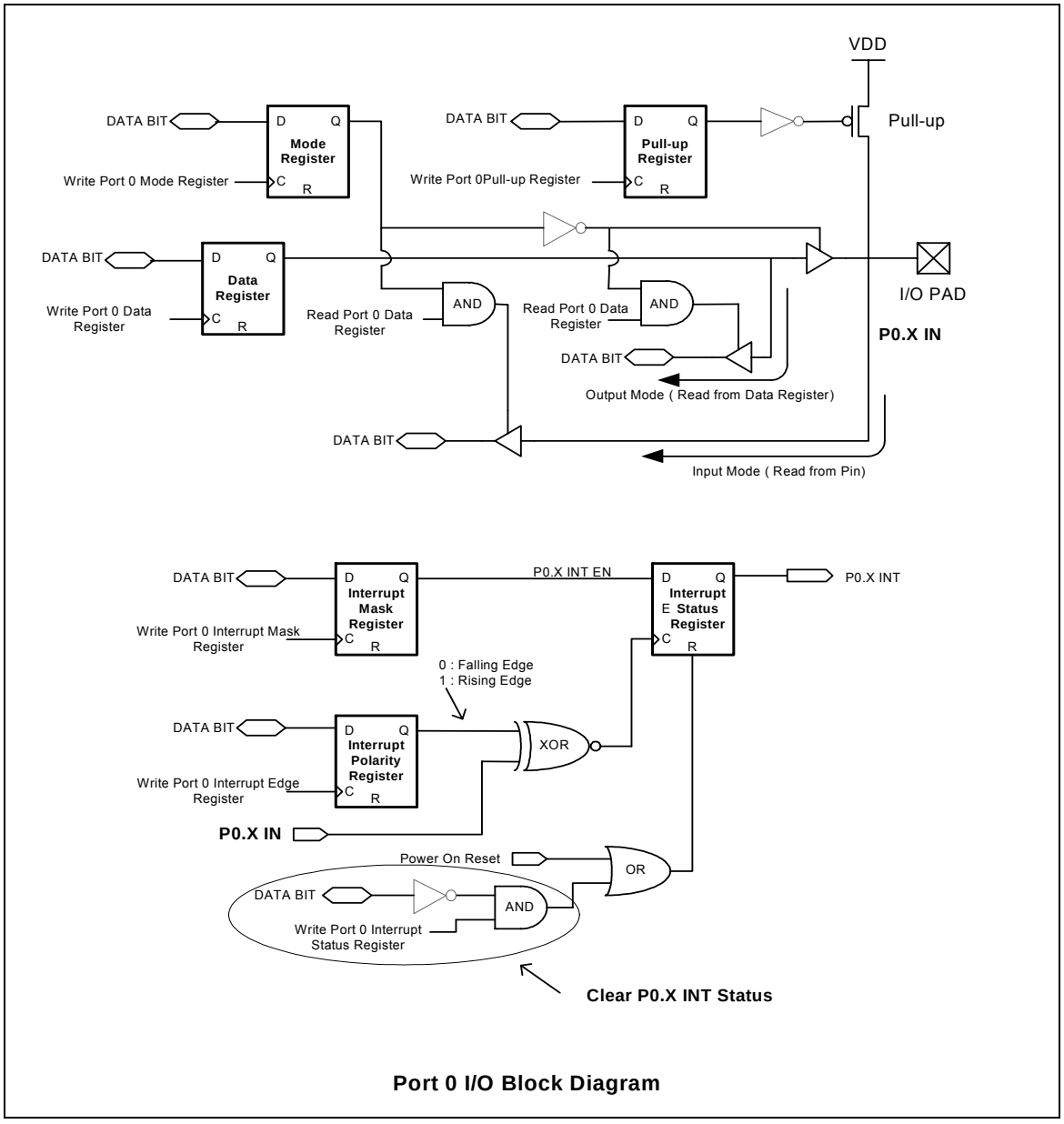
The H6182P has 24 general purpose I/O pins, they are divided to three 8-bits ports (Port 0, 1, 2).

All the I/O pins can be programmed to either input or output mode by individual bit setting of I/O mode registers. Writing and reading the port data register can set the output logic or read the actual logic of pin.

In fact, if the pin is in output mode, writing corresponding bit of data register will output logical high or low, and reading the data register to get the data bit from the data register; In the other, if the pin is input mode, writing the corresponding bit of data register just update the data register bit, and reading the data register to get actual logic of pin.

Each pin of port 0 can be selected to the interrupt source by setting individual bit of P0IMR (Port 0 Interrupt Mask Register), however, the interrupt source pin has to be set to input mode. By the way, each interrupt source pin can be selected to accept the falling or rising edge trigger.

Port 1, 2 is different with port 0, it does not support interrupt source selection, but each pin can be configured to input or output mode, and configured to pull-up or not.



Port 0 I/O Block Diagram

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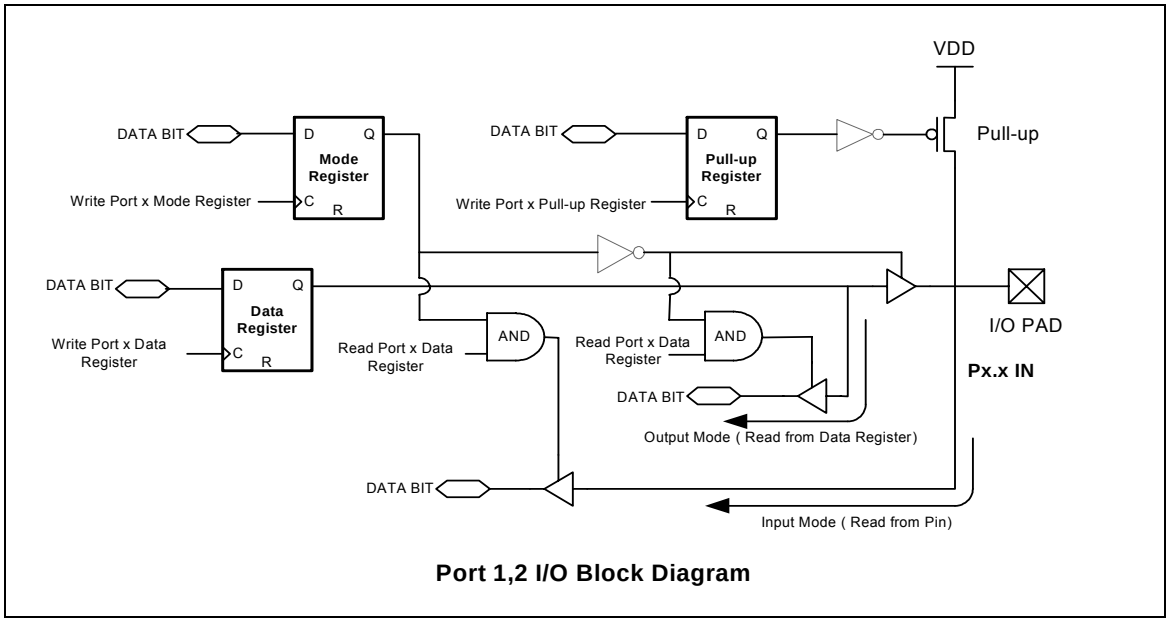

Port 1,2 I/O Block Diagram

1014H: Port 0 I/O Mode Register (P0MR)

1014H , Port 0 I/O Mode Register (P0MR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0[7] Input/Output Select	P0[6] Input/Output Select	P0[5] Input/Output Select	P0[4] Input/Output Select	P0[3] Input/Output Select	P0[2] Input/Output Select	P0[1] Input/Output Select	P0[0] Input/Output Select
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

1: Port 0 pin select input mode.
0: Port 0 pin select output mode.

1015H: Port 0 Pull-up Register (P0PR)

1015H , Port 0 Pull-up Register (P0PR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0[7] Pull-up Enable	P0[6] Pull-up Enable	P0[5] Pull-up Enable	P0[4] Pull-up Enable	P0[3] Pull-up Enable	P0[2] Pull-up Enable	P0[1] Pull-up Enable	P0[0] Pull-up Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

1: The Port 0.X pull-up resistor is enabled.
0: The Port 0.X pull-up resistor is disabled.

1016H: Port 0 Data Register (P0DR)

1016H , Port 0 Data Register (P0DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0[7] Data Bit	P0[6] Data Bit	P0[5] Data Bit	P0[4] Data Bit	P0[3] Data Bit	P0[2] Data Bit	P0[1] Data Bit	P0[0] Data Bit
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write:
1: Port 0 pin output logical high in output mode, but not affect pin in input mode.
0: Port 0 pin output logical low in output mode, but not affect pin in input mode.

Read:
1: Actual pin logical high in input mode, data bit is 1 in output mode.
0: Actual pin logical low in input mode, data bit is 0 in output mode.

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1017H: Port 1 I/O Mode Register (P1MR)

1017H , Port 1 I/O Mode Register (P0MR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P1[7] Input/Output Select	P1[6] Input/Output Select	P1[5] Input/Output Select	P1[4] Input/Output Select	P1[3] Input/Output Select	P1[2] Input/Output Select	P1[1] Input/Output Select	P1[0] Input/Output Select
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

1: Port 1 pin select input mode.
0: Port 1 pin select output mode.

1018H: Port 1 Pull-up Register (P1PR)

1018H , Port 1 Pull-up Register (P1PR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P1[7] Pull-up Enable	P1[6] Pull-up Enable	P1[5] Pull-up Enable	P1[4] Pull-up Enable	P1[3] Pull-up Enable	P1[2] Pull-up Enable	P1[1] Pull-up Enable	P1[0] Pull-up Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1: The Port 1.X pull-up resistor is enabled.
0: The Port 1.X pull-up resistor is disabled.

1019H: Port 1 Data Register (P1DR)

1019H , Port 1 Data Register (P1DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P1[7] Data Bit	P1[6] Data Bit	P1[5] Data Bit	P1[4] Data Bit	P1[3] Data Bit	P1[2] Data Bit	P1[1] Data Bit	P1[0] Data Bit
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write:
1: Port 1 pin output logical high in output mode, but not affect pin in input mode.
0: Port 1 pin output logical low in output mode, but not affect pin in input mode.

Read:
1: Actual pin logical high in input mode, data bit is 1 in output mode.
0: Actual pin logical low in input mode, data bit is 0 in output mode.

1022H: Port 2 I/O Mode Register (P2MR)

1022H , Port 2 I/O Mode Register (P2MR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P2[7] Input/Output Select	P2[6] Input/Output Select	P2[5] Input/Output Select	P2[4] Input/Output Select	P2[3] Input/Output Select	P2[2] Input/Output Select	P2[1] Input/Output Select	P2[0] Input/Output Select
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

1: Port 2 pin select input mode.
0: Port 2 pin select output mode.

1023H: Port 2 Pull-up Register (P2PR)

1023H , Port 2 Pull-up Register (P2PR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P2[7] Pull-up Enable	P2[6] Pull-up Enable	P2[5] Pull-up Enable	P2[4] Pull-up Enable	P2[3] Pull-up Enable	P2[2] Pull-up Enable	P2[1] Pull-up Enable	P2[0] Pull-up Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1: The Port 2.X pull-up resistor is enabled.
0: The Port 2.X pull-up resistor is disabled.

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1024H: Port 2 Data Register (P2DR)

1024H , Port 2 Data Register (P2DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P2[7] Data Bit	P2[6] Data Bit	P2[5] Data Bit	P2[4] Data Bit	P2[3] Data Bit	P2[2] Data Bit	P2[1] Data Bit	P2[0] Data Bit
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write:

1: Port 2 pin output logical high in output mode, but not affect pin in input mode.

0: Port 2 pin output logical low in output mode, but not affect pin in input mode.

Read:

1: Actual pin logical high in input mode, data bit is 1 in output mode.

0: Actual pin logical low in input mode, data bit is 0 in output mode.

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8.6. Timer Control, Timer 0 and Timer 1

The H6182P has two 8-bits timer counters, they are the kind of up-counter, support pre-scale and interrupt events.
Each timer consists of clock pre-scale, 8-bits up-counter, and 8-bits re-load data.
Timer 0 clock source is based on system clock, and has eight pre-scale setting.
Timer 1 clock source can be select from system clock (VCO-DPLL clock) or base clock (VCO clock), and has four pre-scale setting.
Both timer 0 and timer 1 can be set to enable or disable, select clock source and set pre-scale by setting the Timer Mode Register(TMR).

100CH: Timer Mode Register (TMR)

100CH ,Timer Mode Register (TMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 Count Enable	Timer 1 Clock Source select	Timer 1 clock pre-scale		Timer 0 Count Enable	Timer 0 clock pre-scale		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7: Timer 1 Counter Enable/Disable
1: enable Timer 1 count.
0: disable Timer 1 count.

BIT 6: Select timer 1 clock source from system clock or base clock.
1: Select system clock.
0: Select base clock.

BIT 5~4: Timer 1 Clock Pre-Scale

Select Timer 1 clock source.

T1C[1]	T1C[0]	Timer 1 Clock Source
0	**0**	Clock Source (System Clock or Base Clock)
0	**1**	Clock Source / 8
1	**0**	Clock Source / 64
1	**1**	Clock Source / 1024

BIT 3: Timer 0 Counter Enable/Disable
1: enable Timer 0 count.
0: disable Timer 0 count.

BIT 2~0: Timer 0 Clock Pre-Scale

Select Timer 0 clock source.

T0C[2]	T0C[1]	T0C[0]	Timer 0 Clock Source
0	**0**	**0**	System Clock
0	**0**	**1**	System Clock / 4
0	**1**	**0**	System Clock / 16
0	**1**	**1**	System Clock / 64
1	**0**	**0**	System Clock / 256
1	**0**	**1**	System Clock / 1024
1	**1**	**0**	System Clock / 4096
1	**1**	**1**	System Clock / 16384

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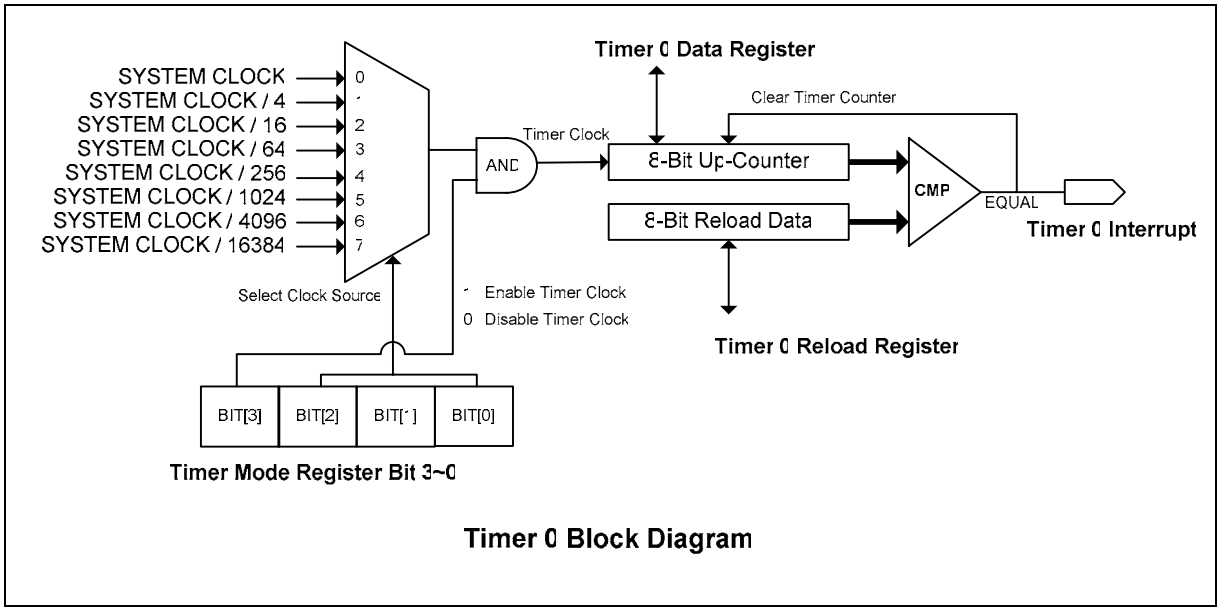

Timer 0 Block Diagram

100DH: Timer 0 Reload Register (T0RR)

100DH , Timer 0 Reload Register (T0RR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 0 counter reload value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write this register to set timer 0 counter reload counter value.

Since the timer 0 counter is an up-counter, the counter will be automatically cleared while the timer counter reaches the reload value. And the 'clear event' also sets the timer 0 interrupt status.

100EH: Timer 0 Data Register (T0DR)

100EH , Timer 0 Data Register (T0DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 0 Counter Value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write this register to set initiate value of timer 0 counter, and read this register to get timer 0 counter current values.

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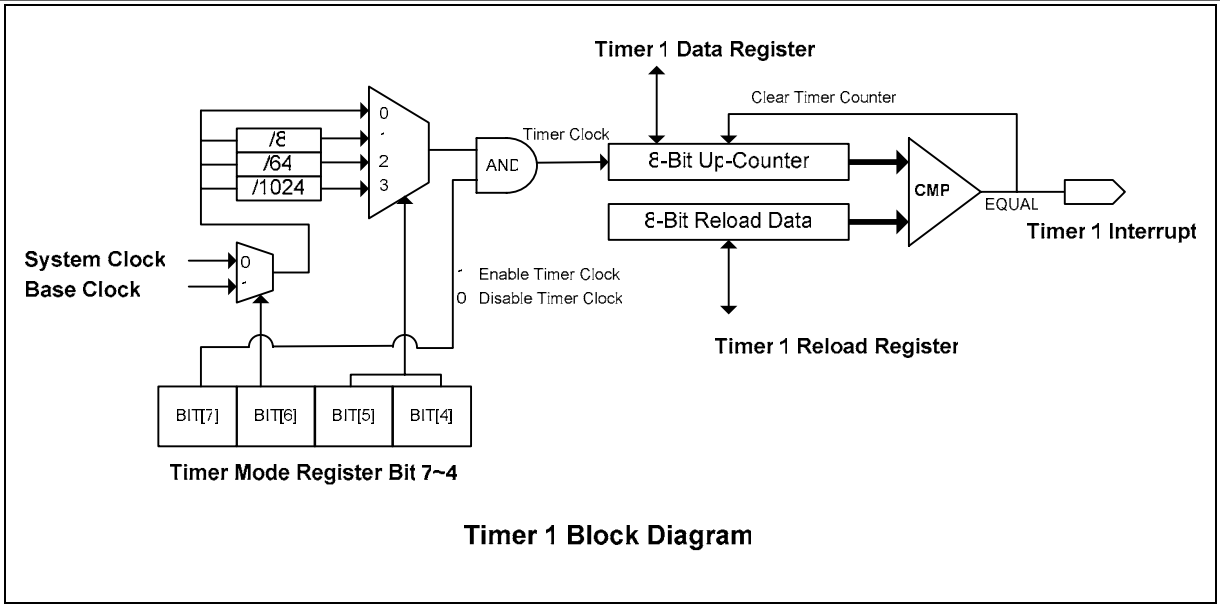

Timer 1 Block Diagram

100FH: Timer 1 Reload Register (T1RR)

100FH , Timer 1 Reload Register (T1RR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 counter reload value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write this register to set timer 1 counter reload counter value.
Since the timer1 counter is an up-counter, the counter will be auto cleared while the timer counter reaches the reload value. The ”clear event” also sets the timer 1 interrupt status.

1010H: Timer 1 Data Register (T1DR)

1010H , Timer 1 Data Register (T1DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 Counter Value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write this register to set timer 1 counter initiated value, and read this register to get timer 1 counter current value.

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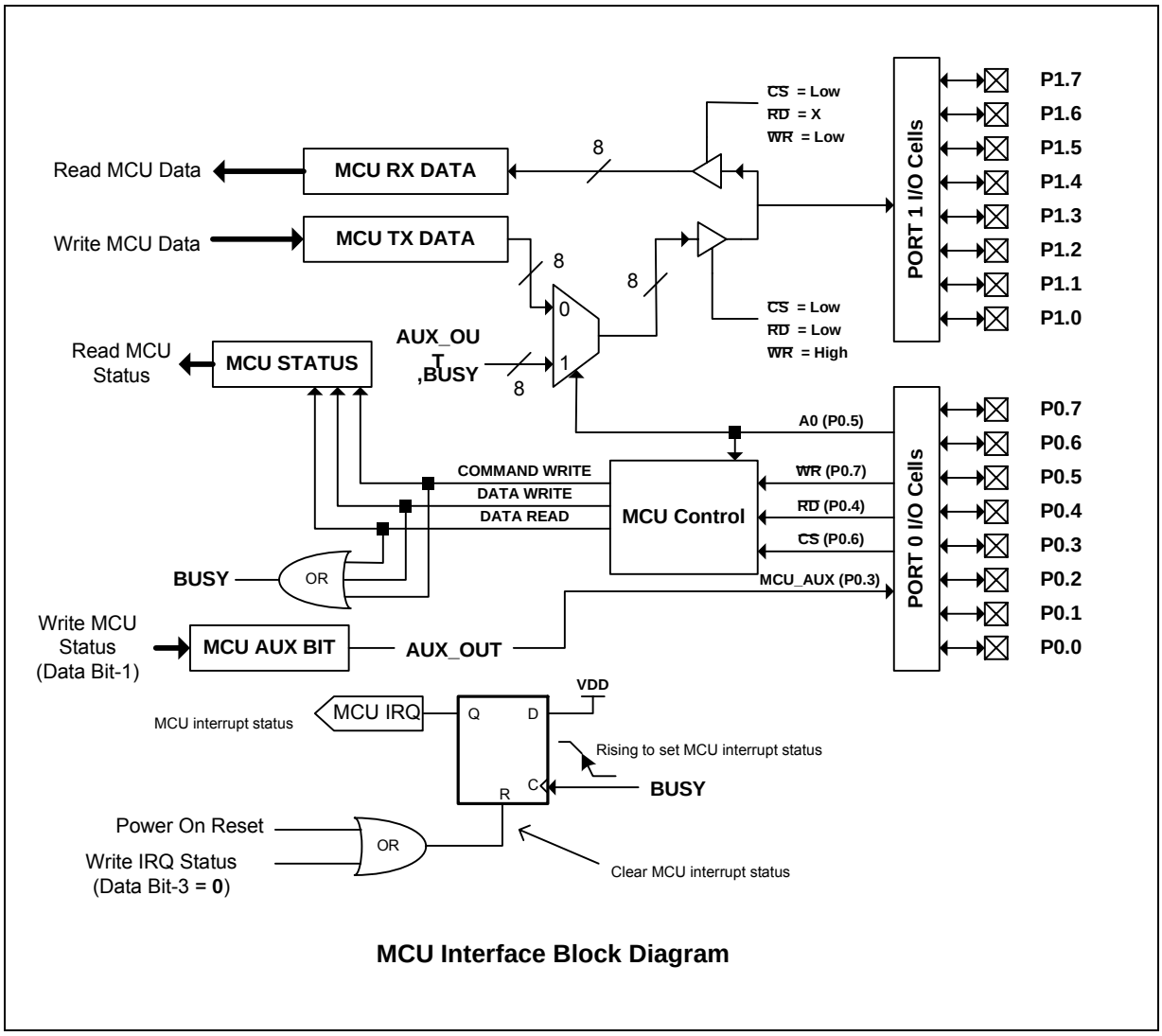
8.7. MCU Interface Control

The H6182P supports an 8-bit parallel data communication interface, this interface is functional option with I/O; the data bus uses the Port-1, and the control pins are /CS, /WR, /RD, A0, MCU_AUX that use the Port-0.7 ~ Port-0.3.

As the logical definition, the MCU interface has two communicating ports; they are command port and data port, that is identified with A0, and the data bus direction is identified by combination of /WR and /RD.



MCU Interface Block Diagram

Because the MCU interface is defined to configure the H6182P to be a slave device, we usually identify the operations by host-MCU operations.

There are four operations identified:

(1) COMMAND READ: The host-MCU reads data from command port of H6182P, check interface busy.

(2) COMMAND WRITE: The host-MCU writes data to command port of H6182P.

(3) DATA READ: The host-MCU reads data from data port of H6182P.

(4) DATA WRITE: The host-MCU writes data to data port of H6182P.

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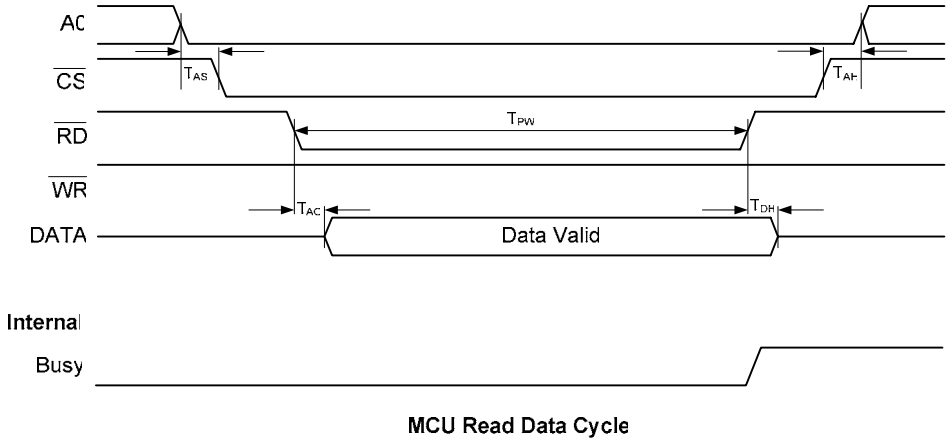
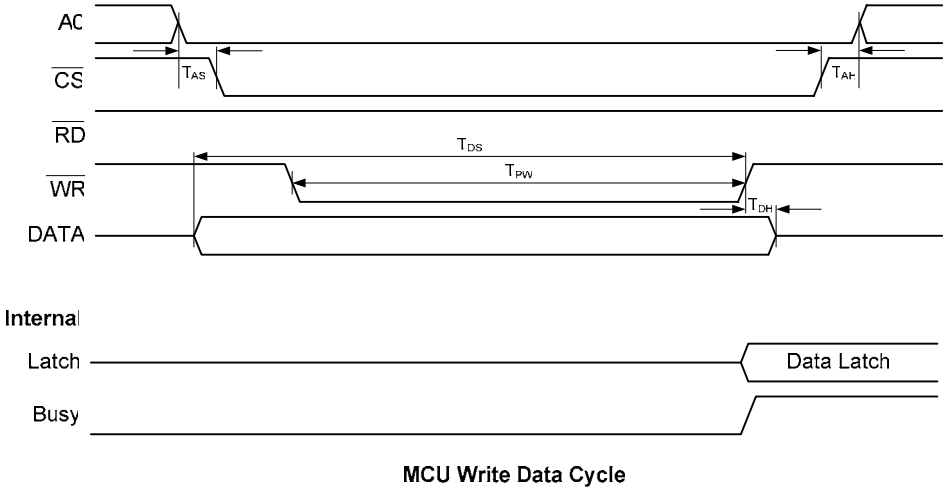
The following table given the combinational operations about host-MCU accessing the MCU interface:

/CS	A[0]	/RD	/WR	MCU Operations
0	0	0	1	Read Data Port
0	0	1	0	Write Data Port
0	1	0	1	Read Command Port
0	1	1	0	Write Command Port
1	X	X	X	None

The Host-MCU Access Timing via MCU Interface



MCU Read Data Cycle



MCU Write Data Cycle

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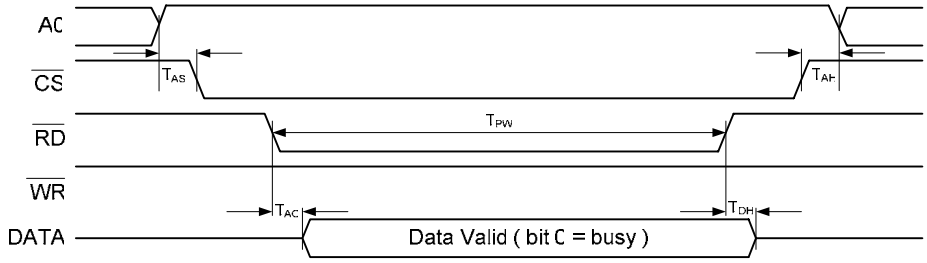
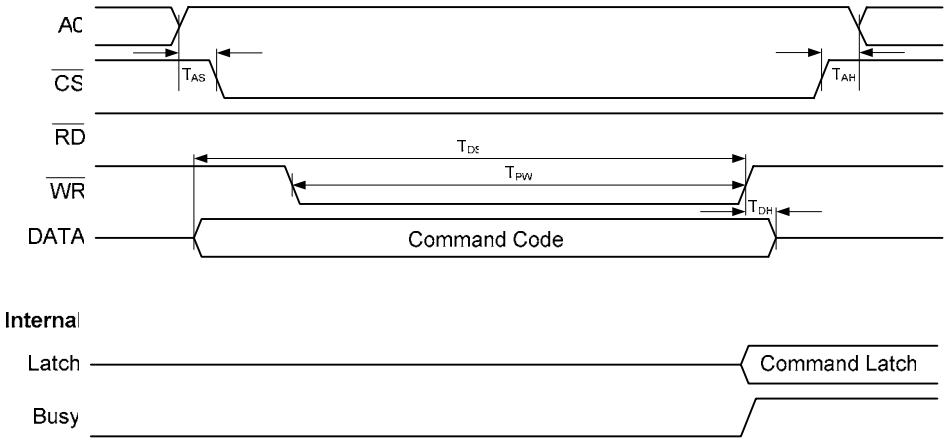


Internal

Busy Not affect

MCU Read Command Cycle



MCU Write Command Cycle

101AH : MCU Status Register (MCUSR)

101AH , MCU Status Register (MCUSR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name						Data Read Status	Data Write Status (MCU AUX)	Command Write Status
Read/Write	X	X	X	X	X	R	R/W	R
Reset	X	X	X	X	X	0	0	0

Read this register to get the MCU data transferring status.

Status Bit 2~0:

001: host-MCU writes command to MCU RX.

010: host-MCU writes data to MCU RX.

100: host-MCU has read data from MCU TX.

These three bits are exclusive true, and any of these bits is set to “1” for indicating busy of the MCU interface. If the bit-3 of Interrupt Request Enable Register (IRQER) is set to “1” to enable the MCU interrupt and enable the Jupiter’s interrupt flag, then any change of these three statuses will cause the Jupiter to process interrupt.

The H6182P’s firmware can check these three bits to process the necessary MCU data transferring. After the firmware processes the corresponding tasks, clear these three bits to “0” by write “0” to bit-3 of Interrupt Status Register (IRQSR) for next data transferring.

Writing this register, only bit 1 is effective, and it directed affects the MCU_AUX (P0.3).

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1: MCU_AUX output logical high.

0: MCU_AUX output logical low.

101BH: MCU Data Register (MCUDR)

101BH ,MCU Data Register (MCUDR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	MCU TX, RX data buffer							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Read this register to get the MCU RX data buffer that is data or command from host-MCU.

Before accessing this register, check MCU Status Register BIT 2~0 to process the necessary read/write:

001: host-MCU write command, read MCU RX to get command.

010: host-MCU write data, read MCU RX to get data.

100: host-MCU has read data from MCU TX, in other word, MCU TX empty.

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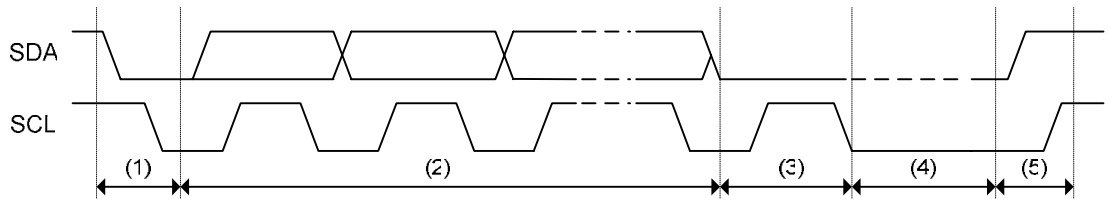
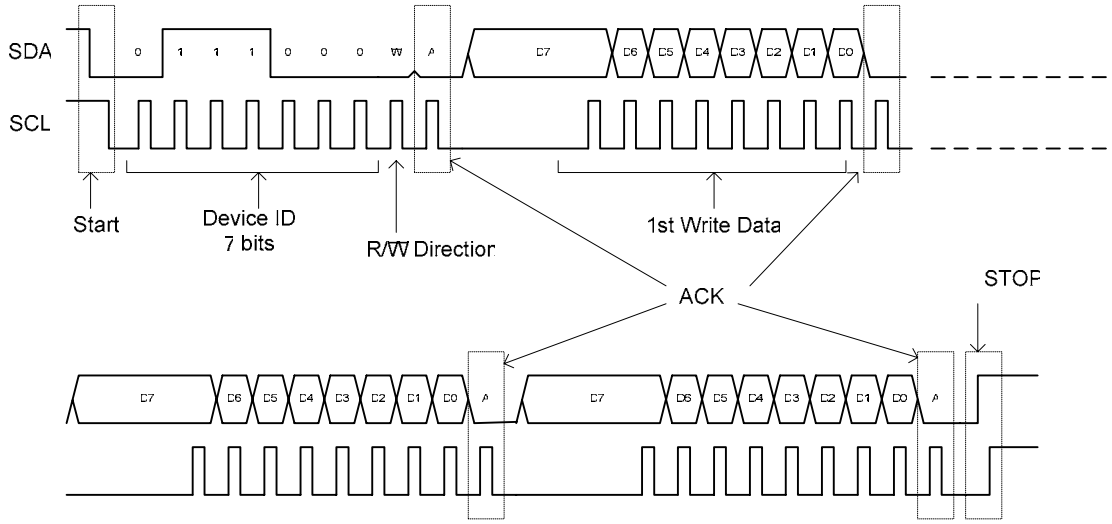
8.8. 2-wired Serial Bus Interface

The 2-wire serial bus function consists of two bi-direction communication pins, they are clock pin (SCL) and data pin (SDA). The serial bus interface in H6161P only supports device (slave) mode, and it supports programmable slave device ID (Address) that is 7 bits but the MSB is fixed to 0.



(1) Start stage
(2) 7-bit ID (Address) + 1-bit direction (R/W) stage
(3) ACK/NACK acknowledge or none-acknowledge stage
(4) device hold SCL low not ready for next data transaction
(5) Stop stage



Two-wire serial bus timming conditions

101CH: Serial Bus Mode Register (SBUSMR)

101CH , Serial Bus Mode Register (SBUSMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Acknowledge (ACK) Enable/Disable	General Call Enable/Disable	Device ID (Device Address) Bit 5..0					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7: Acknowledge (ACK) Enable/Disable
0: Set the device none-acknowledge (NACK) to the serial bus of data transmission.
1: Set the device acknowledge (ACK) to the serial bus of data transmission.

BIT 6: General Call Enable/Disable
0: Set the device NACK to the host's general call.

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1: Set the device ACK to the host's general call.

BIT 5~0: Device ID (Device Address) Bit 5~0

Set the device address.

In fact, the 2-wired serial bus function of H6161P supports 7-bit device ID (Address) to configure the different ID, and the 7th bit of ID (Address) is fix "0". Thus, the device ID can be configured from 0000000b to 0111111b.

101DH: Serial Bus Status Register (SBUSSR)

101DH , Serial Bus Status Register (SBUSSR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Data Transfer Complete	Reserved			Host Acknowledge	General Call	1st Data	Transfer Direction
Read/Write	R	X	X	X	R	R	R	R
Reset	0	0	0	0	0	0	0	0

BIT 7: Data Transfer Completed Flag

0: None data received in SBUS RX and none SBUS TX have been transmitted.

1: Data received complete in SBUS RX or SBUS TX data has been transmitted complete.

BIT 6~4: reserved (unused)

BIT 3: Host Acknowledge Flag

0: The host responses the none-acknowledge (NACK) after the SBUS TX data transmission is completed.

1: The host responses the acknowledge (ACK) after the SBUS TX data transmission is completed.

It can be known by checking this bit whether host read stage is completed or not

If the host acknowledges the data transmission, the device (H6161P) has to set next transmitting data to the SBUS TX for host's next reading. Otherwise, the host set none-acknowledge, that means the stage of host read is completed.

BIT 2: General Call Flag

0: The received ID (Address) is not a general call.

1: The received ID (Address) is a general call.

The general call ID is 0001111b, the device can be configured to process general call if it is necessary.

About the general call procedure, please refer to the standard I2C specification.

BIT 1: First Data Transfer Flag

0: The data received is not the 1st data after received device ID.

1: The data received is the 1st data after received device ID.

BIT 0: Data Transfer Direction Flag

0: The received ID means host write completion that gets the received data by reading SBUS RX.

1: The received ID means host read request, the system should process transmitting data.

101EH: Serial Bus Transmit Data Register (SBUSTX)

101EH , Serial Bus Transmit Register (SBUSTX)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Transmit Data Byte							
Read/Write	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Write this register to transmit data to host.

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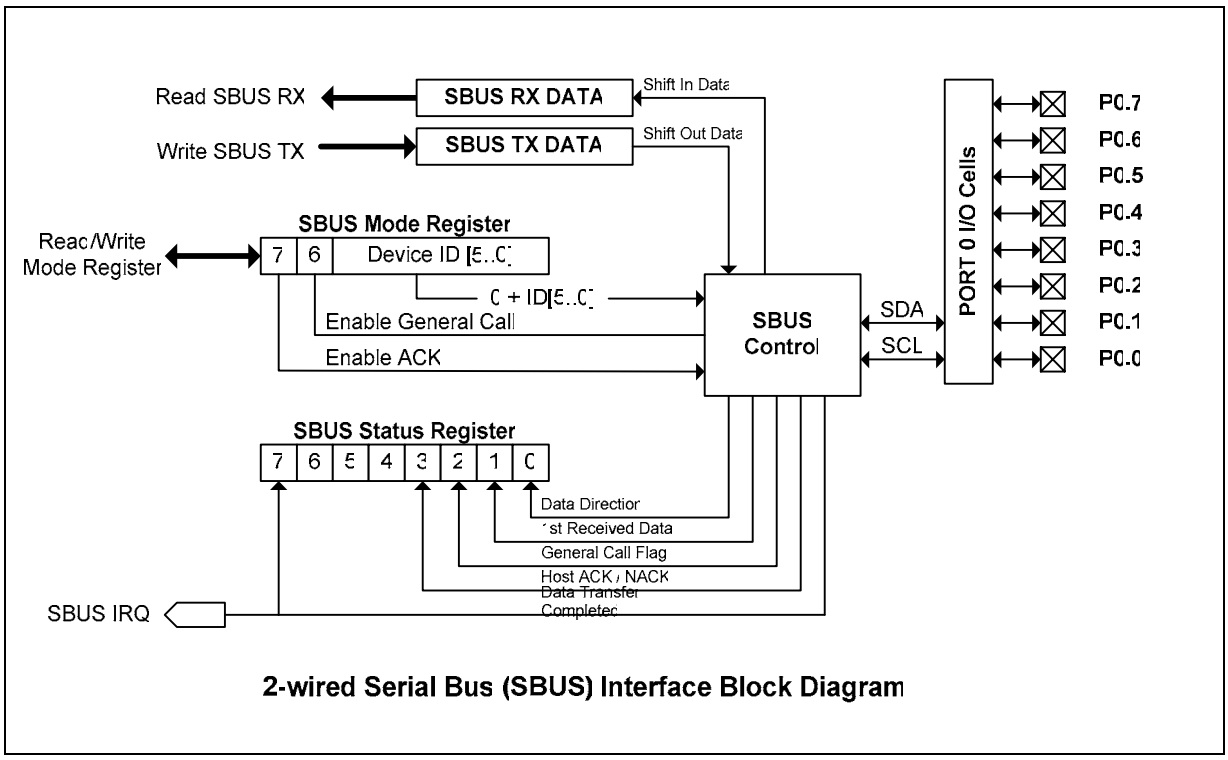
101FH: Serial Bus Receive Data Register (SBUSRX)

101FH , Serial Bus Receive Data Register (SBUSRX)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Receive Data Byte							
Read/Write	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Read this register to get received data.



2-wired Serial Bus (SBUS) Interface Block Diagram

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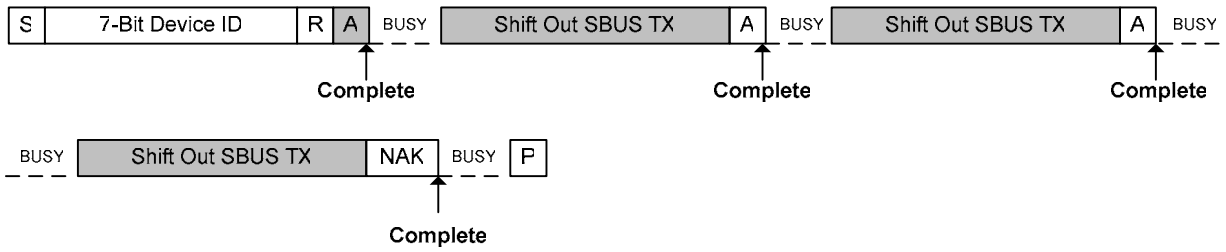
To check serial bus status register for processing the data transferring, there are two methods to identify the serial bus events, the one is to configure interrupt enable register to process event by interrupt, the other is to poll the bit-7 of serial bus status register (data transfer completed flag).

There are 3 data transferring completed events (these events cause interrupt if using interrupt method):

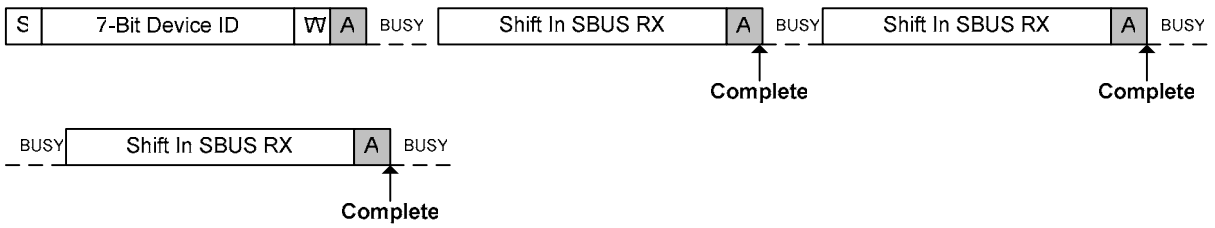
(1) Host completed device-ID-read, if the device ID is matched.
(2) Host completed data-read.
(3) Host completed the data-write.

Please refer to the following figure.

Host Read From Device



Host Write to Device



S	Serial Bus Start Stage
P	Serial Bus Stop Stage
R	Serial Bus read
W	Serial Bus write
A	Serial Bus Host Acknowledge
NAK	Serial Bus Host None-Acknowledge
A	Serial Bus Device Acknowledge
NAK	Serial Bus Device None-Acknowledge
BUSY	Serial Bus Device Busy SCL low

Serial Bus Data Transferring Completed Status

Configure and Control Serial Bus Steps:

(1) To configure the device ID by initiating the SBUS Mode Register.
(2) Enable the serial bus interrupt by setting the bit-4 of 'Interrupt request enable register' (IRQER, 1001H).
(3) Check bit-4 of 'Interrupt status register' (IRQSR, 1002H) in interrupt service routine (ISR).
(4) Check serial bus status register if interrupt status bit of serial bus in IRQSR is asserted.
(5) Process the necessary data transferring by checking serial bus status register.
(6) Clear serial bus interrupt status (bit-4 of interrupt status register) after completing the process.

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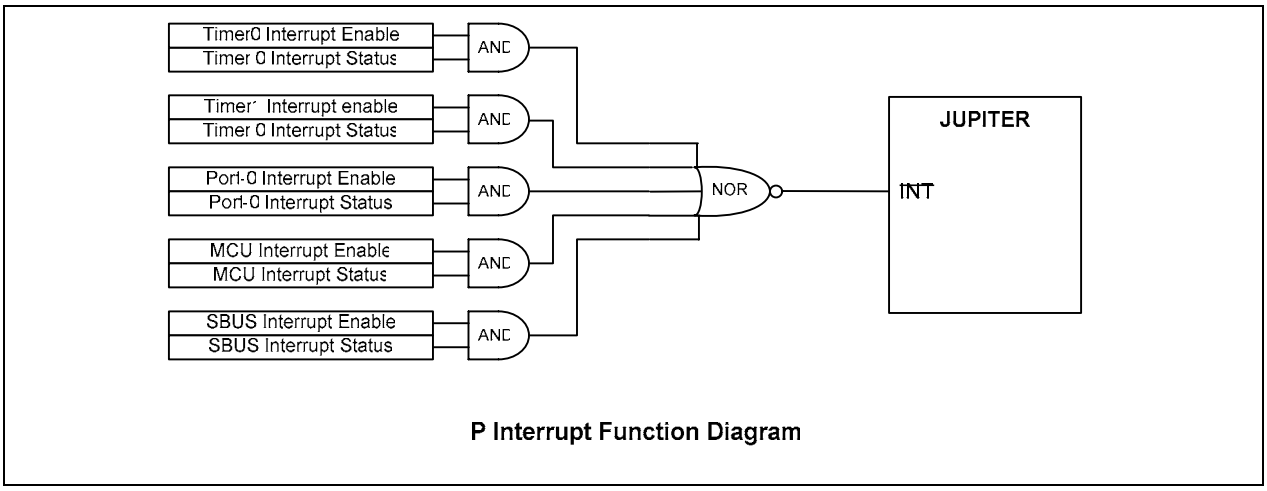
8.9. Interrupts Control

The H6182P has five Interrupt sources:

(1) Timer-0 Interrupt.
(2) Timer-1 Interrupt.
(3) Port-0 Interrupt.
(4) MCU I/F Interrupt.
(5) Serial Bus Interrupt.

The (1) and (2) are both programmable timer interrupts, (3) is also called GPIO interrupt and can be configured to select external interrupt sources. The (4) and (5) are communicational interrupt for interfacing with external controller.



P Interrupt Function Diagram

1001H: Interrupt Request Enable Register (IRQER)

1001H , Interrupt Request Enable Register (IRQER)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name				SBUS Interrupt Enable/Disable	MCU Interrupt Enable/Disable	Port-0 Interrupt Enable/Disable	Timer 1 Interrupt Enable/Disable	Timer 0 Interrupt Enable/Disable
Read/Write	X	X	X	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	0	0	0	0	0

BIT 7~5: Reserved

BIT 4: Enable/Disable Serial Bus Interrupt.
0: Disable
1: Enable

BIT 3: Enable/Disable MCU Interface Interrupt.
0: Disable
1: Enable

BIT 2: Enable/Disable Port-0 Interrupt.
0: Disable
1: Enable

BIT 1: Enable/Disable Timer 1 Interrupt.
0: Disable
1: Enable

BIT 0: Enable/Disable Timer 0 Interrupt.
0: Disable
1: Enable

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1002H: Interrupt Status Register (IRQSR)

1002H , Interrupt Status Register (IRQSR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name				SBUS Interrupt Status	MCU Interrupt Status	Port-0 Interrupt Status	Timer 1 Interrupt Status	Timer 0 Interrupt Status
Read/Write	X	X	X	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	0	0	0	0	0

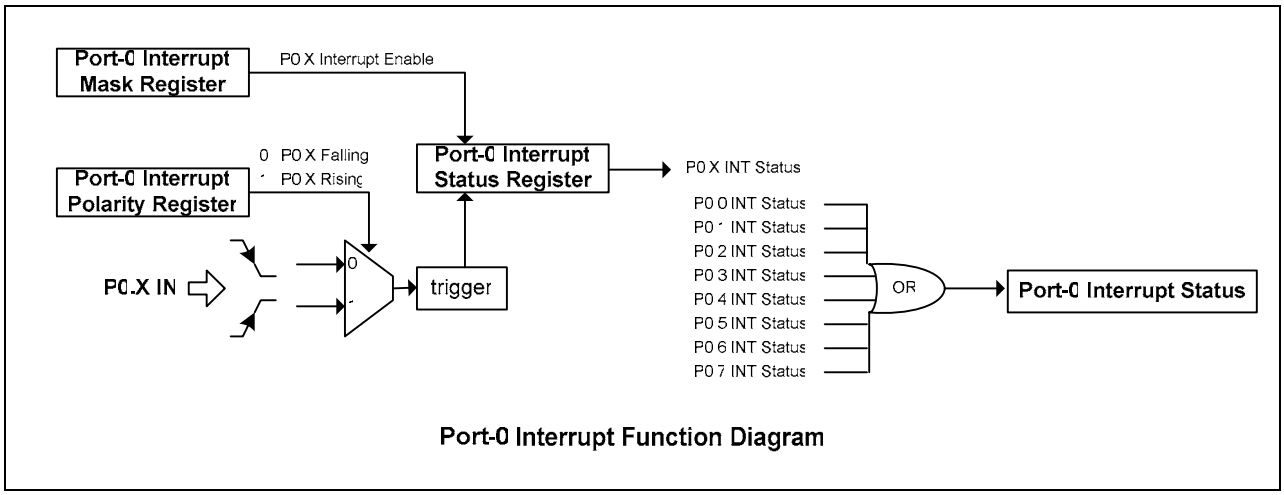
Check each interrupt status of this register in the interrupt service routine, then do the necessary procedures.
After completed the corresponding interrupt task, clear the interrupt status by write 0 to the corresponding bit.

Note that write 1 to the status bits will not affect the status bits, only write 0 to clear the status bits, usually, it was called EOI (End of Interrupt).

The Port-0 Interrupt (GPIO Interrupt), External Interrupt Sources

The H6182P features the eight external interrupt sources by configuring the Port-0. Each Port-0 I/O can be configured individually to accept the logical rising or falling signal.

Since the interrupt sources are from the external events, the Port-0 I/O pins have to be configured to input mode. About the Port-0 I/O mode setting, please refer to the previous GPIO control. This section will discuss the Port-0 Interrupt registers.



Port-0 Interrupt Function Diagram

1011H: Port-0 Interrupt Mask Register (P0IMR)

1011H , Port-0 Interrupt Mask Register (P0IMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0.7 Interrupt Enable/Disable	P0.6 Interrupt Enable/Disable	P0.5 Interrupt Enable/Disable	P0.4 Interrupt Enable/Disable	P0.3 Interrupt Enable/Disable	P0.2 Interrupt Enable/Disable	P0.1 Interrupt Enable/Disable	P0.0 Interrupt Enable/Disable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7 ~ 0: P0.7 ~ P0.0 interrupt enable or disable
0: Disable the P0.X interrupt.
1: Enable the P0.X interrupt.

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1012H: Port-0 Interrupt Polarity Register (P0IPR)

1012H , Port-0 Interrupt Polarity Register (P0IPR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0.7 Interrupt Polarity	P0.6 Interrupt Polarity	P0.5 Interrupt Polarity	P0.4 Interrupt Polarity	P0.3 Interrupt Polarity	P0.2 Interrupt Polarity	P0.1 Interrupt Polarity	P0.0 Interrupt Polarity
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7 ~ 0: P0.7 ~ P0.0 interrupt polarity select
0: select falling edge.
1: select rising edge.

1013H: Port-0 Interrupt Status Register (P0ISR)

1013H , Port-0 Interrupt Status Register (P0ISR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	P0.7 Interrupt Status	P0.6 Interrupt Status	P0.5 Interrupt Status	P0.4 Interrupt Status	P0.3 Interrupt Status	P0.2 Interrupt Status	P0.1 Interrupt Status	P0.0 Interrupt Status
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BIT 7 ~ 0: P0.7 ~ P0.0 interrupt assert or not
0: Nothing.
1: Indicate the P0.X interrupt asserts.

There is only one interrupt entry for H6182P system, and all the interrupt events are identified by reading and checking the interrupt status register. For serving the interrupts, enable the Jupiter's interrupt (PSR.3 = 1 or STI) and enable the desired interrupt source by setting the interrupt enable register.

When the internal interrupt signal is asserted, it will cause Jupiter to serve the interrupt. PSR will be pushed to stack automatically and then the interrupt flag of PSR will be cleared to prevent the re-entry of interrupt. After that, the next normal instruction address will also be pushed to stack and the program counter will be changed to the interrupt entry address that is defined in absolute address FEH and FFH.

The firmware has to initiate the interrupt entry address before enabling the interrupt, and all the Jupiter's registers are considered to be saved by pushing to stack, then checking the interrupt status for each interrupt sources. In addition, do not forget to clear the status after completing the interrupt tasks.

Please refer to the following interrupt service routine:

```
; ============================================================================
; INTERRUPT SERVICE ROUTINE.
; ============================================================================
IRQ_PROCESS             FUNCTION
                        PUSHA                                   ; BACKUP A,X,PTR REGISTER.
; ============================================================
; CHECK_T0_ISR_PROC
                        JBZ     [IRQ_STATUS], 00000001B,@T0_ISR_QUIT
                        MOVE    [IRQ_STATUS], 11111110B         ; T0 ISR EOI
                        ; ----------------------------------
                        ; DO TIMER0 INTERRUPT SERVICE ROUTINE.
                        ; ----------------------------------
@T0_ISR_QUIT
; ============================================================
; CHECK_T1_ISR_PROC
                        JBZ     [IRQ_STATUS], 00000010B,@T1_ISR_QUIT
                        MOVE    [IRQ_STATUS], 11111101B         ; T1 ISR EOI
                        ; ----------------------------------
                        ; DO TIMER1 INTERRUPT SERVICE ROUTINE.
                        ; ----------------------------------
```


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```
@T1_ISR_QUIT
; ============================================================
; CHECK_P0_ISR_PROC
                        JBZ     [IRQ_STATUS], 00000100B,@P0_ISR_QUIT
                        ; ----------------------------------
                        ; DO PORT0 INTERRUPT SERVICE ROUTINE.
                        ; ----------------------------------
                        MOVE    [PORT0_IRQ_STATUS],0
                        MOVE    [IRQ_STATUS], 11111011B             ; P0 ISR EOI
@P0_ISR_QUIT
; ============================================================
; CHECK_MCU_ISR_PROC
                        JBZ     [IRQ_STATUS], 00001000B,@MCU_ISR_QUIT
                        MOVE    [IRQ_STATUS], 11110111B             ; MCU ISR EOI
                        ; ----------------------------------
                        ; DO MCU INTERFACE INTERRUPT SERVICE ROUTINE.
                        ; ----------------------------------
@MCU_ISR_QUIT
; ============================================================
; CHECK_SBUS_ISR_PROC
                        JBZ     [IRQ_STATUS], 00010000B,@SBUS_ISR_QUIT
                        MOVE    [IRQ_STATUS], 11101111B             ; SBUS ISR EOI
                        ; ----------------------------------
                        ; DO SBUS INTERFACE INTERRUPT SERVICE ROUTINE.
                        ; ----------------------------------
@SBUS_ISR_QUIT
; ============================================================
                        POPA                                        ; RESTORE PTR,X,A REGISTER.
                        RETI
IRQ_PROCESS             ENDF
```

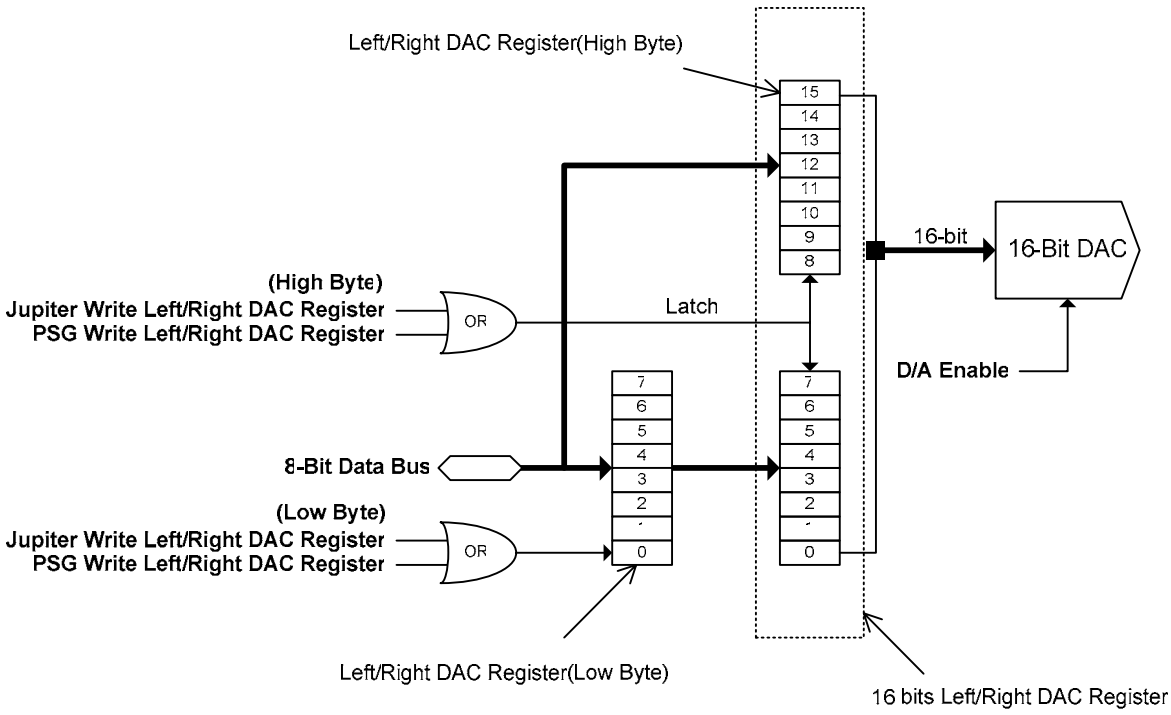
8.10. Audio Control

The H6182P supports two 16-bit DAC (digital-to-analog converter) output functions (output on AUDIO_R and AUDIO_L), and the DAC is utilized with 2-2R resistors network.

These two DACs are controlled by both left/right DAC register and PSG. When the H6161P serves the DAC output control, the PSG function has to be disabled. On the other hand, the H6182P shall not affect the DAC while the PSG is operating.

Thus, we define two ways for controlling the D/A outputs, one is direct D/A controlling that is directly controlled by Jupiter (DSP-Core), and the other way is controlled by PSG.

Since the H6182P is generally designed to audio application (Speech/Melody), it also features the EQ-OP and a 0.5W speaker amplifier to drive the audio output signal.



Left/Right D/A and Data Register Block Diagram

1004H, 1005H: Left DAC Data Register (LDACR)

1004H ~ 1005H, Left DAC Data Register (LDACR)																
	1005H High Byte							1004H Low Byte								
Bit No.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	16-bit Left DAC Data															
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write this 16-bit register to output analog signal

Since the H6182P is an 8-bit bus system, writing the low byte only latches data to the buffer and won't affect the DAC output. The 16-bit DAC output will be updated together after writing the high byte.

1006H, 1007H: Right DAC Data Register (RDACR)

1006H ~ 1007H, Right DAC Data Register (RDACR)																
	1007H High Byte							1006H Low Byte								
Bit No.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	16-bit Right DAC Data															
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write this 16-bit register to output analog signal

Since the H6182P is an 8-bit bus system, writing the low byte only latches date to the buffer and won't affect the DAC output, the 16-bit DAC output will be updated together after writing the high byte.

1021FH Watch-Dog Timer Control Register (WDCR)

021FH Watch-Dog Timer Control Register, (WDCR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Watch-Dog Timer Clock Pre-scale				Watch-Dog Control Mode			
Read/Write	W	W	W	W	W	W	W	W
Reset	0	0	0	0	1	1	1	1

[7:4] Watch-Dog Timer Clock Pre-scale: These bits are used to set the value of pre-scale that divides the R/C base Block as below:

Base Clock / (pre-scale + 1)

Watch-Dog Timer will reset the CPU if watch-dog timer is not cleared within 65536 Watch-Dog Timer clock cycles. The system control registers is not affected by this watch-dog timer reset and keep the same values.

[3:0] Watch-Dog Control Mode: These bit are used to control the watch-dog timer as below:

0 = Disable.
5 = Clear.
F = Enable.

This register is write-only.

Default :

Fastest : Pre-scale = 0

1/(Base Clock / (0+1)) *65536 = 0.83ns*65536 = 54.395ms

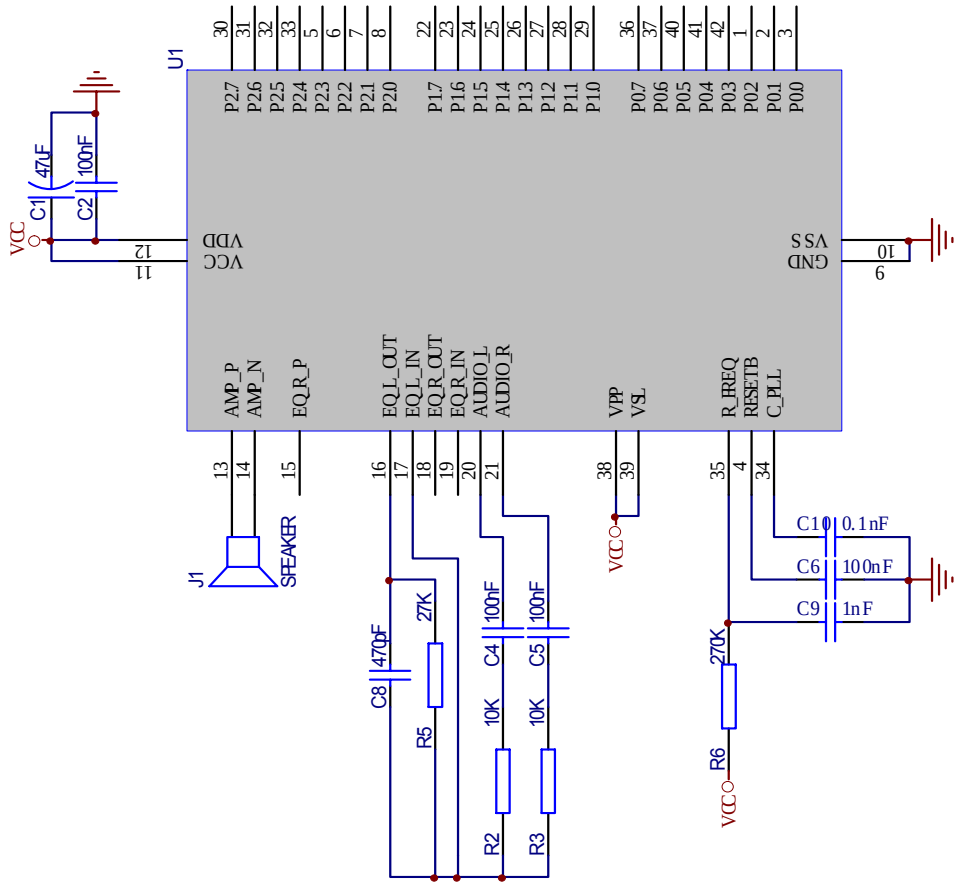
8.11. Power down Control

The power down control part is used to stop the system clock (VCO-DPLL) of H6182P for power saving. Note that the GPIO driving loading should be taken into consideration and analog OP and speaker amplifier should be turned off respectively as well to save the power.

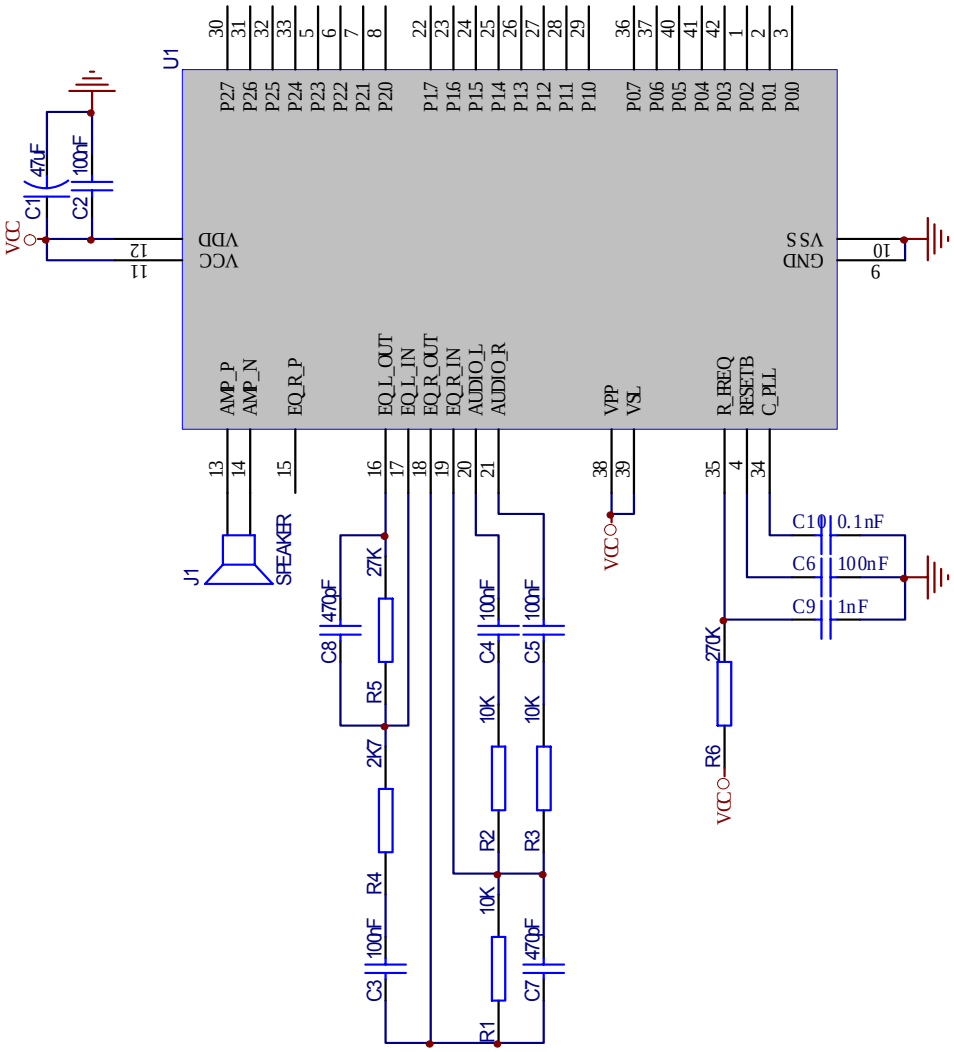
The following shows the example code to set the H6182P to power down mode:

```
POWER_DOWN
        CLI
        CALL    AMP_OFF_PROC

        MOVE    [PORT0_PH_MODE], 11111111B      ; ENABLE P07~P00 INTERNAL PULL-HIGH.
        MOVE    [PORT1_PH_MODE], 11111111B      ; ENABLE P17~P10 INTERNAL PULL-HIGH.
        MOVE    [PORT0_IRQ_MASK],11111111B      ; P07~P00 INTERRUPT MASK = NONE.
        MOVE    [PORT0_IRQ_EDGE],00000000B      ; P07~P00 INTERRUPT EDGE = FALLING.
        MOVE    [PORT0_IRQ_STATUS],0            ; CLEAR P07~P00 INTERRUPT STATUS.
        MOVE    [IRQ_STATUS],0                  ; CLEAR INTERRUPT STATUS.
        MOVE    [IRQ_ENABLE],00000100B          ; PORT0 INTERRUPT ENABLE.
        NOP
ENTRY_SLEEP
        MOVE    [SYSTEM_CONTROL],0              ; BASE_CLOCK OFF & ALL EQUIPMENT OFF.
        NOP
        NOP
P0_PIN_CHANGE_WAKEUP
        CLI
        MOVE    [IRQ_ENABLE],0
        MOVE    [IRQ_STATUS],0
        MOVE    [PORT0_IRQ_STATUS],0

        MOVE    A,MTR_VALUE                     ; MTR_VALUE = 6CH(Recommend)
        MOVE    MTR,A
        MOVE    [PSG_MTR],A
        MOVEW   [IRQ_VECTOR], IRQ_PROCESS
        MOVE    A,0FDH
        MOVE    SP,A                            ; RE-INITIAL THE STACK POINTER.
        MOVE    [DPLL_CONTROL], DPLL_VALUE
        CALL    WAIT_CLOCK_STABLE
        MOVEW [BASE_CLOCK_FACTOR], (BASE_CLOCK / 1000000) * 1024
```

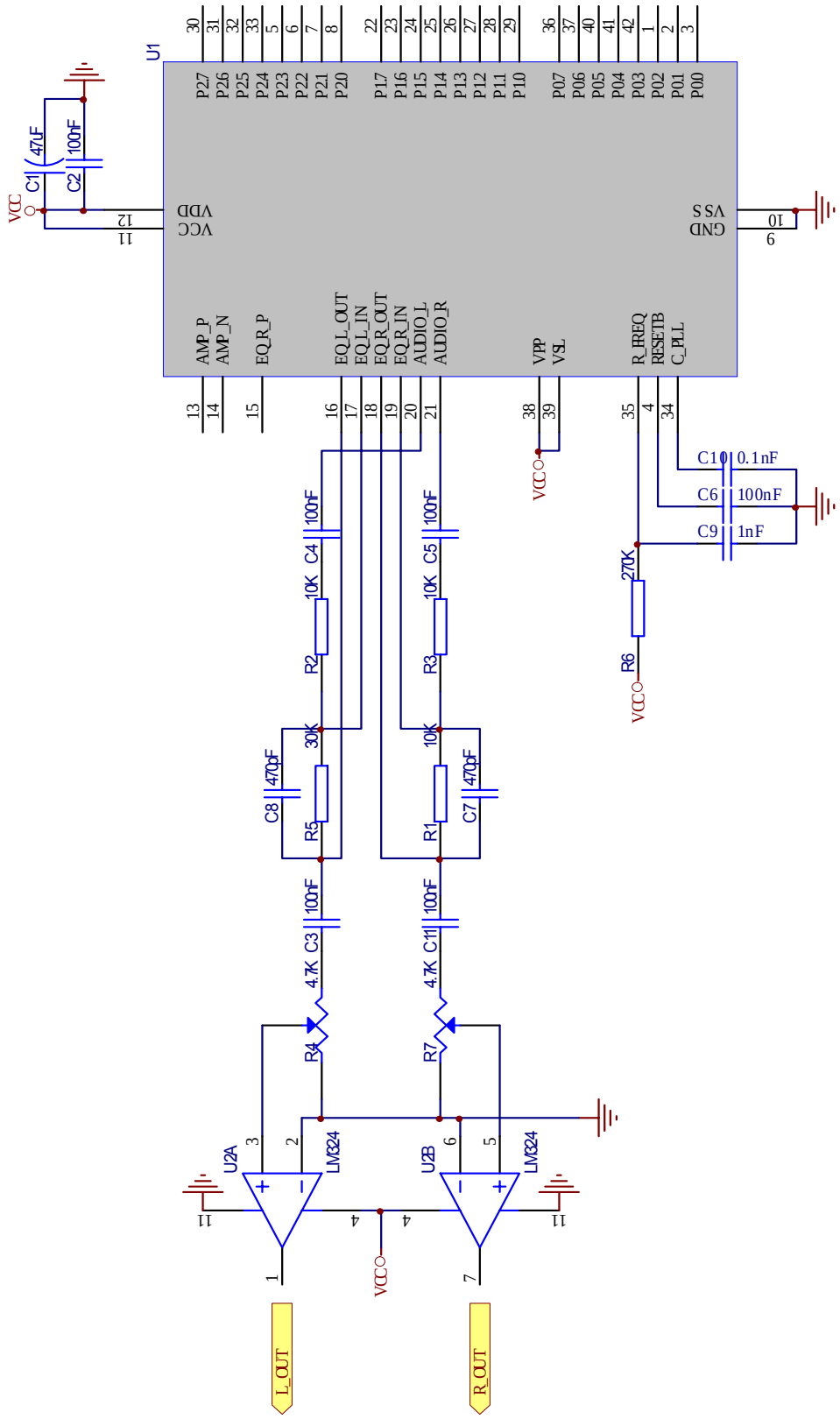
9. Application Circuit



Mono one step EQ



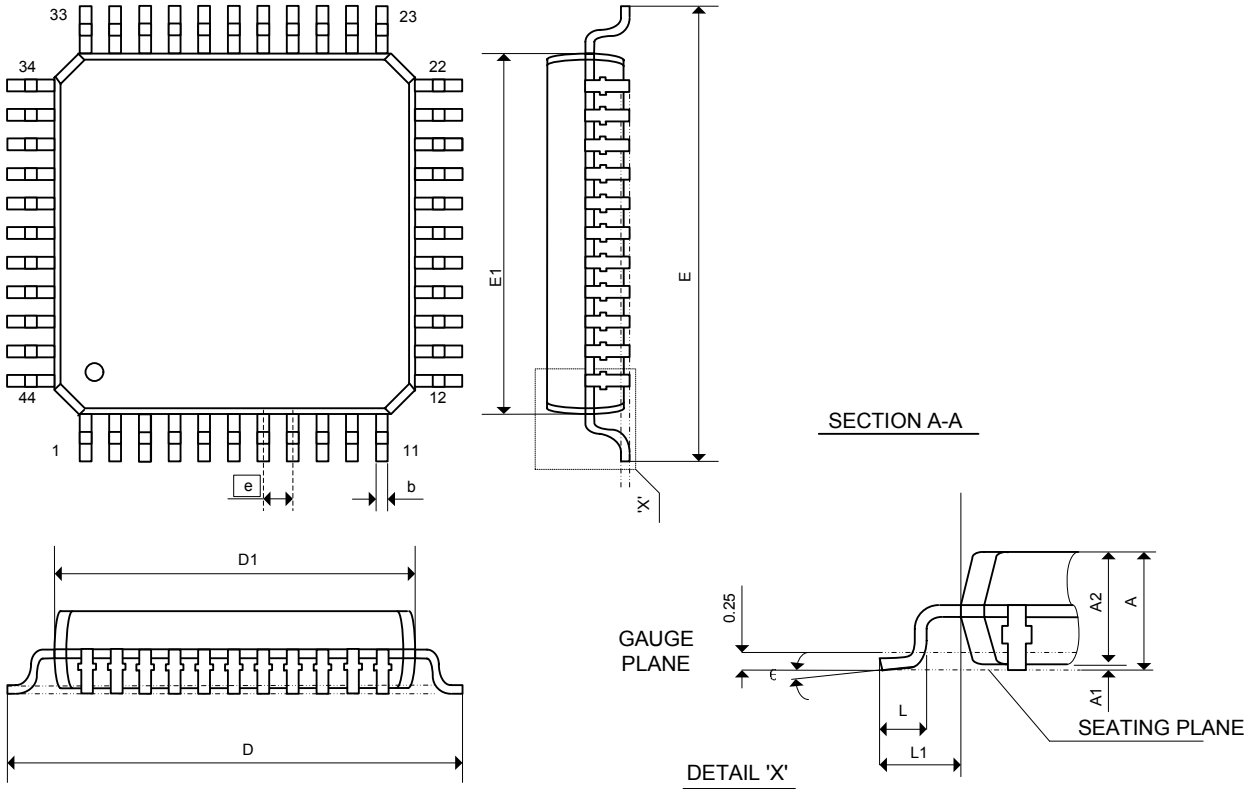
Mono two step EQ



Stereo Output

10. Packages Outline

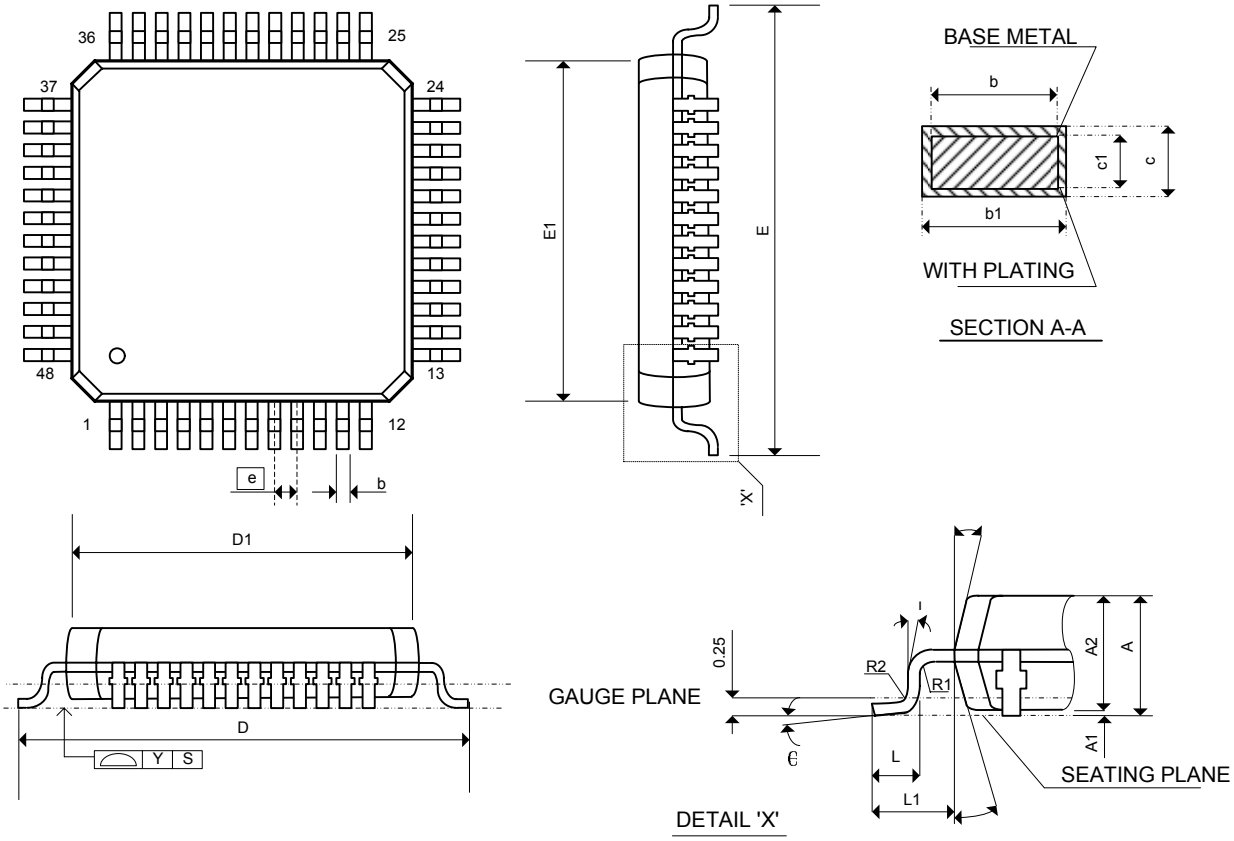
Package Drawings	44-Lead Plastic Quad Flat Package (**QFP**) **QFP 44 (10 x 10 mm)**



SYBBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	2.30	-	-	91
A1	0.05	0.10	0.15	2	4	6
A2	2.00	2.10	2.20	79	83	87
b	0.29	-	0.37	11	-	15
b1	0.28	0.30	0.33	11	12	13
c	0.15	-	0.20	6	-	8
c1	0.14	0.15	0.16	6	6	6
D	13.00	13.20	13.40	512	520	528
D1	9.80	10.00	10.20	386	394	402
E	13.00	13.20	13.40	512	520	528
E1	9.80	10.00	10.20	386	394	402
e	0.80 BSC			31 BSC		
L	0.55	0.70	0.85	22	28	33
L1	1.60 REF			63 REF		
θ	0°	-	8°	0°	-	8°

NOTE:
1. REFER TO HTFQ0441010B
2. ALL DIMENSION IN MILLIMETERS.

Package Drawings	48-Lead Plastic Low Profile Quad Flat Package (**LQFP**) **LQFP 48 (7x7 mm)**



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.60	-	-	63
A1	0.05	0.15	0.25	2	6	10
A2	1.30	1.40	1.50	51	55	59
b	0.19	-	0.27	7	-	11
b1	0.18	0.20	0.23	7	8	9
c	0.13	-	0.18	5	-	7
c1	0.12	0.13	0.14	5	5	6
D	8.80	9.00	9.20	346	354	362
D1	6.80	7.00	7.20	268	276	283
E	8.80	9.00	9.20	346	354	362
E1	6.80	7.00	7.20	268	276	283
e	0.50 BSC			20 BSC		
L	0.35	0.50	0.65	14	20	26
L1	1.00 REF			39 REF		
θ	0°	-	8°	0°	-	8°

NOTE:
1. REFER TO HTFL0480707
2. ALL DIMENSION IN MILLIMETERS.